MULTI-EFFECT PROCESSOR

EMP700

SERVICE MANUAL

EMP700

■ **CONTENTS**（目次）

LM 011095

YAMAHA CORP.
HAMAMATSU, JAPAN
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IMPORTANT NOTICE

This manual has been provided for the use of authorized Yamaha Retailers and their service personnel. It has been assumed that basic service procedures inherent to the industry, and more specifically Yamaha Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components and failure of the product to perform as specified. For these reasons, we advise all Yamaha product owners that all service required should be performed by an authorized Yamaha Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification, recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of Yamaha are continually striving to improve Yamaha products. Modifications are, therefore, inevitable and changes in specification are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit OFF during disassembly and parts replacement. Recheck all work before you apply power to the unit.

This product uses a lithium battery for memory back-up.

WARNING: Lithium batteries are dangerous because they can be exploded by improper handling. Observe the following precautions when handling or replacing lithium batteries.

- Leave lithium battery replacement to qualified service personnel.
- Always replace with batteries of the same type.
- When installing on the PC board, solder using the connection terminals provided on the battery cells. Never solder directly to the cells. Perform the soldering as quickly as possible.
- Never reverse the battery polarities when installing.
- Do not short the batteries.
- Do not attempt to recharge these batteries.
- Do not disassemble the batteries.
- Never heat batteries or throw them into fire.

ADVARSEL!

Lithiumbatteri. Eksplosionsfare.

Udskiftning må kun foretages af en sagkyndig, og som beskrevet i servicemanualen.

WARNING: CHEMICAL CONTENT NOTICE!

The solder used in the production of this product contains LEAD. In addition, other electrical/electronic and/or plastic (where applicable) components may also contain traces of chemicals found by the California Health and Welfare Agency (and possibly other entities) to cause cancer and/or birth defects or other reproductive harm.

DO NOT PLACE SOLDER, ELECTRICAL/ELECTRONIC OR PLASTIC COMPONENTS IN YOUR MOUTH FOR ANY REASON WHAT SO EVER!

Avoid prolonged, unprotected contact between solder and your skin! When soldering, do not inhale solder fumes or expose eyes to solder/flux vapor!.

If you come in contact with solder or components located inside the enclosure of this product, wash your hands before handling food.

■ SPECIFICATIONS

• Inputs	2 channels, 1/4" phone jack, impedance greater than 500KΩ.
• Outputs	2 channels, 1/4" phone jack, impedance 1KΩ.
• Input/Output Level	–20dB/+4dB switchable.
• Sampling Frequency	44.1 kHz.
• Quantization	16 bits.
• Frequency Response	20 Hz ... 20 kHz.
• Dynamic Range	Greater than 85 dB, effect off.
• T.H.D	Less than 0.1% @ 1 kHz.
• Internal Memory	90 presets in ROM, 50 user RAM.
• External Memory	RAM (50 programs) cards, optional.
• Power Consumption	US & Canadian model: 120V AC, 10 watts. General model: 220 ... 240V AC, 10 watts.
• Dimensions (W x H x D)	480 x 44 x 216.2 mm. (18-7/8" x 1-3/4" x 8-1/2")
• Weight	2.9 kg. (6 lbs. 6 oz)

■ 総合仕様

電気特性

周波数特性	20Hz～20kHz
ダイナミックレンジ	85dB（@エフェクトOFF時）
歪率	0.03%（@1kHz）

インプット（INPUT）

チャンネル数	2cH
入力レベル	+4dBm／−20dBm
入力インピーダンス	500kΩ以上

アウトプット（OUTPUT）

チャンネル数	2cH
出力レベル	+4dBm／−20dBm
出力インピーダンス	1kΩ

AD／DA変換

チャンネル数	2cH
サンプリング周波数	44.1kHz
量子化ビット数	16bit

メモリー

プリセットプログラムエリア
No.0～90（No.0はイニシャルデータ）
ユーザーズプログラムエリア
No.1～50
別売メモリーカードプログラムエリア
No.1～50

MIDIコントロール

プログラムチェンジ、ノートオン、コントロールチェンジ、バルクダンプ機能

フロントパネル

スイッチ	POWER
コントロール	INPUT LEVEL（L，R）
キー	ソフトキー（▲）、アップダウンキー（▲，▼）、MEMORY、PARAM（DYN，REV）、UTILITY、RECALL、STORE、ASSIGN、BYPASS
ディスプレイ	16文字×2行LCD(LED照明付き) 2桁7セグメントLED（メモリーナンバー） 2cH、2素子LED（レベルメーター） 3素子LED（PRESET、USER、CARD表示） 1素子LED（MIDI表示） 6素子LED（モード表示）
スロット	メモリーカード

リアパネル

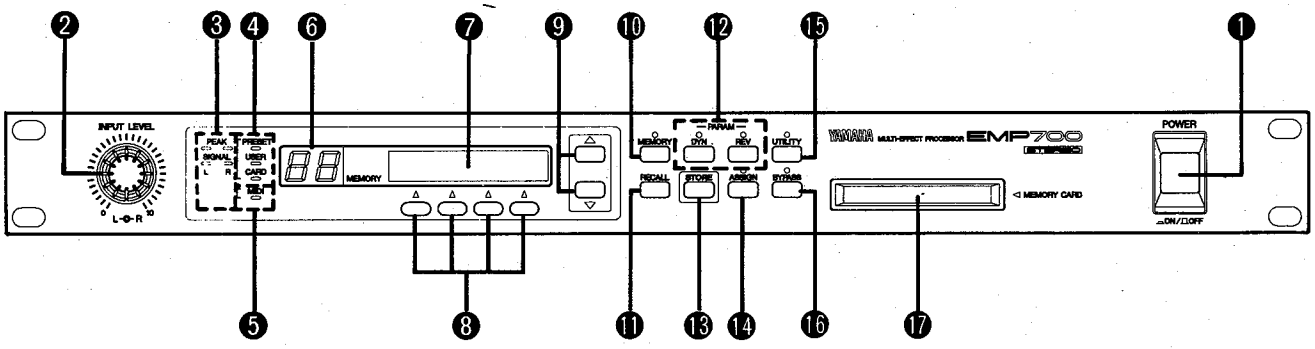
端子	INPUT L／R（フォーンジャック×2） OUTPUT L／R（フォーンジャック×2） MIDI IN，THRU／OUT（DIN 5pin×2） TAP TEMPO／BYPASS（フォーンジャック）
スイッチ	入出力レベル切換スイッチ（+4dB／−20dB） MIDI THRU／OUT切換スイッチ

電源	AC100V、50／60Hz
消費電力	8.5W
寸法	480(W)×44(H)×216.2(D) mm
重量	2.9kg

※0dB＝0.775Vr.m.s.

■ PANEL LAYOUT（パネルレイアウト）

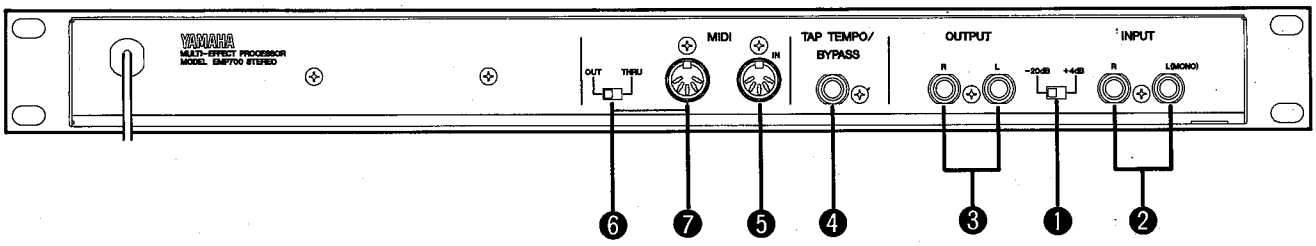
● Front Panel（フロントパネル）



❶ Power Switch
❷ INPUT LEVEL Controls
❸ SIGNAL and PEAK Indicators
❹ PRESET, USER and CARD Indicators
❺ MIDI Indicators
❻ LED MEMORY Number Display
❼ Liquid Crystal Display
❽ Assignable Function Keys
❾ [▲] and [▼] Keys
❿ [MEMORY] Mode Keys & Indicator
⓫ [RECALL] Key
⓬ PARAM Keys & Indicators (DYN, REV)
⓭ [STORE] Key
⓮ [ASSIGN] Key & Indicator
⓯ [UTILITY] Mode Key & Indicator
⓰ [BYPASS] Key & Indicator
⓱ MEMORY CARD Slot

❶POWERスイッチ
❷INPUT LEVELコントロール
❸SIGNAL, PEAKインジケーター
❹メモリーエリアインジケーター（PRESET,USER,CARD）
❺MIDIインジケーター
❻メモリーNo.ディスプレイ
❼LCDディスプレイ
❽ソフトキー
❾アップダウンキー
❿メモリー選択キーとインジケーター
⓫メモリーRECALLキー
⓬パラメーターエディットキー（DYN,REV）
⓭メモリーSTOREキー
⓮ASSIGNキーとインジケーター
⓯UTILITYキーとインジケーター
⓰BYPASSキーとインジケーター
⓱メモリーカードスロット

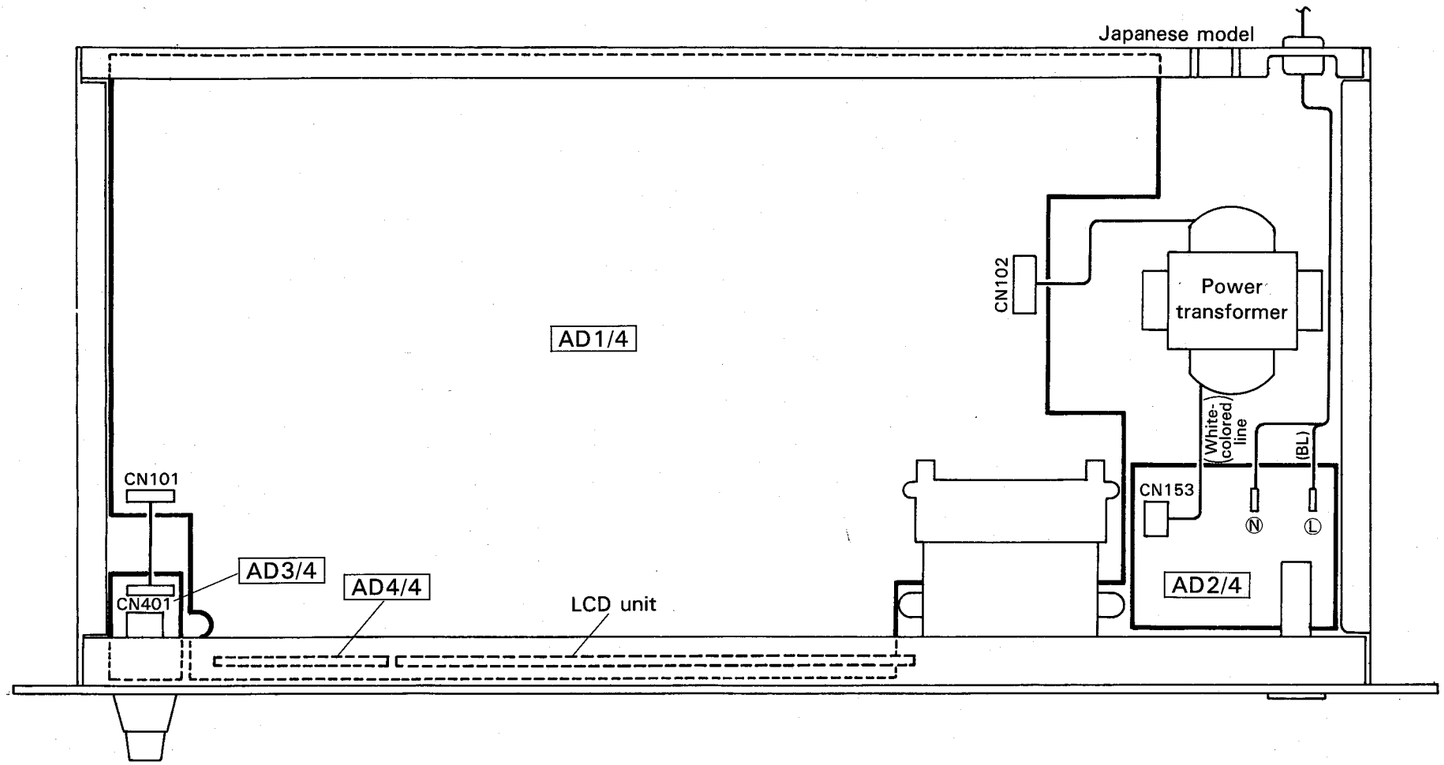
● Rear Panel（リアパネル）



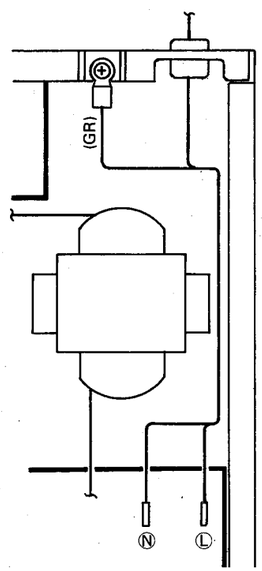
❶ −20dB/+4dB Input/Output Level Switch
❷ INPUT R & L (MONO) Jacks
❸ OUTPUT R and OUTPUT L Jacks
❹ TAP TEMPO/BYPASS Jack
❺ MIDI IN Connector
❻ MIDI OUT/THRU Switch
❼ MIDI OUT/THRU Connector

❶入出力レベル切換スイッチ（−20dB/+4dB）
❷INPUT端子（R,L(MONO)）
❸OUTPUT端子（L,R）
❹フットスイッチ端子（TAP TEMPO/BYPASS）
❺MIDI IN端子
❻MIDI OUT/THRU切換スイッチ
❼MIDI OUT/THRU端子

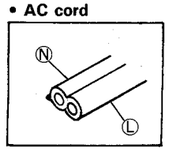
■CIRCUIT BOARD LAYOUT（ユニットレイアウト）



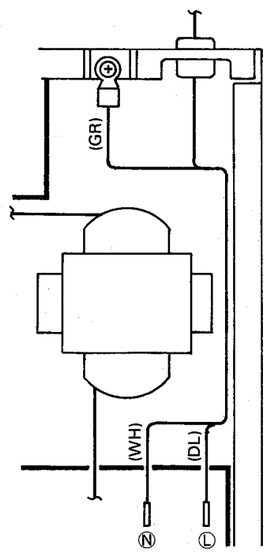
U.S. and General export (110V) models



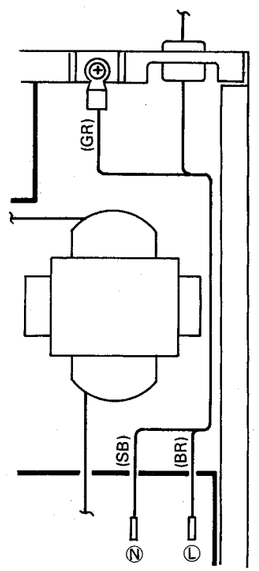
• AC cord



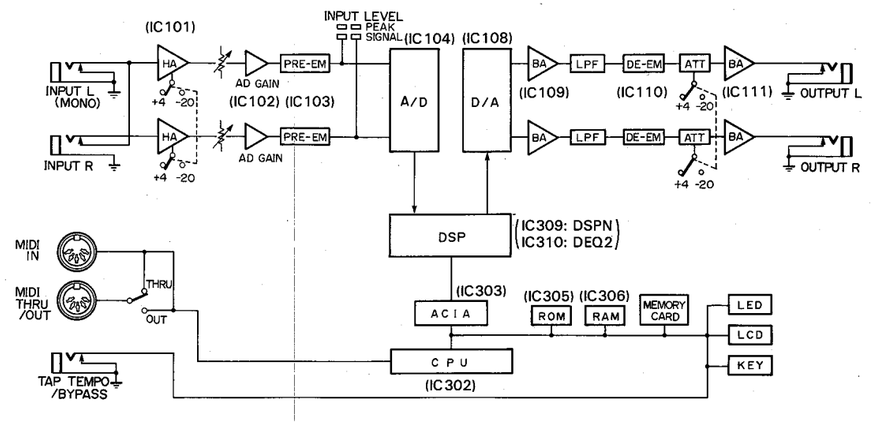
Canadian model



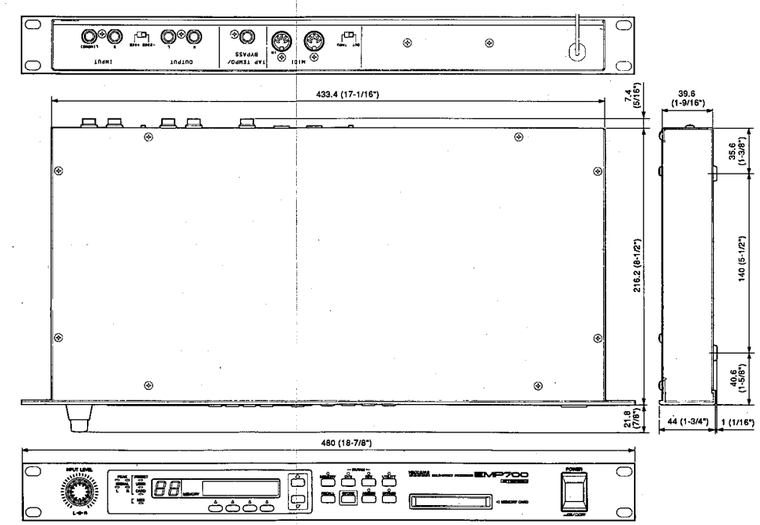
European model



■BLOCK DIAGRAM（ブロック図）



■DIMENSIONS（寸法図）



Unit=mm (inch)
（単位）

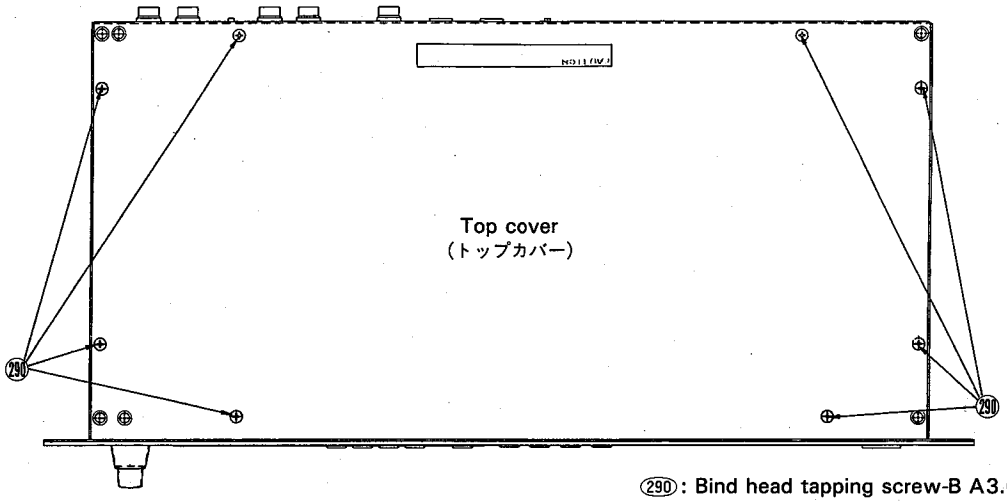
■ DISASSEMBLY PROCEDURE（分解手順）

1. Top Cover Removal

1-1. Remove the eight (8) screws marked as (290) in the figure, then the top cover can be removed. (Fig. 1)

1．トップカバーの外し方

1-1. (290)のネジ8本を外し、トップカバーを外します。（図1）



(290): Bind head tapping screw-B A3.0×6 FCM3BL

(Fig. 1)

2. Front Panel Assembly Removal

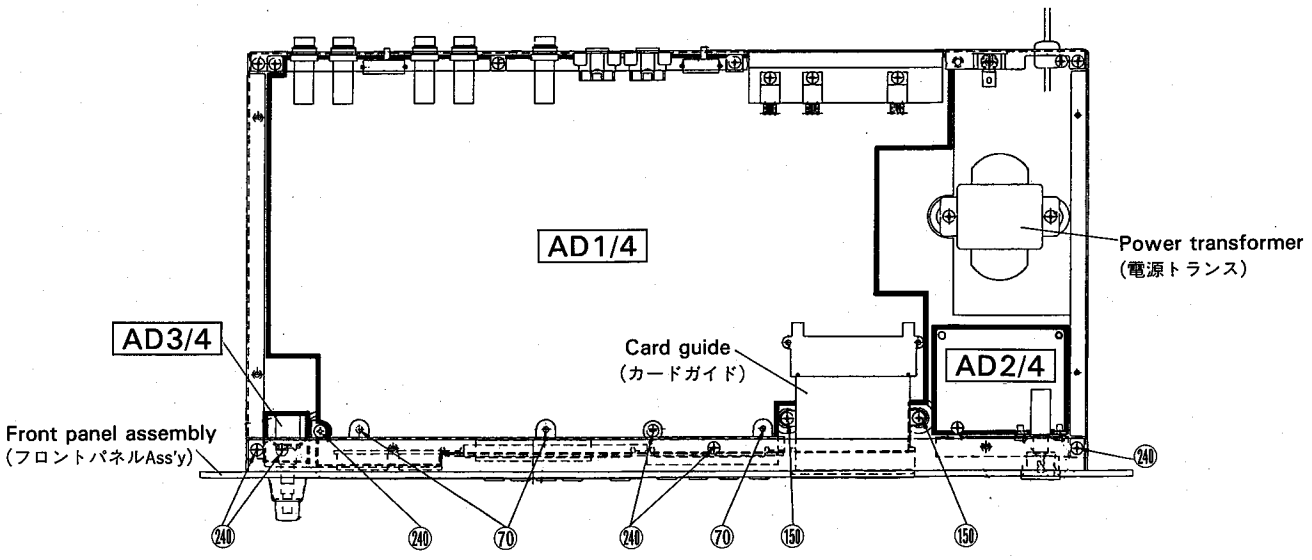
2-1. Remove the top cover. (see procedure 1)

2-2. Remove the six (6) screws marked (240), then the front panel assembly can be removed. (Fig. 2)

2．フロントパネルAss'yの外し方

2-1. トップカバーを外します。（1項参照）

2-2. (240)のネジ6本を外し、フロントパネルAss'yを外します。（図2）



(Fig. 2)

(70): Bind head tapping screw-B A3.0×6 FCM3BL
(150): Bind head tapping screw-B A3.0×6 FCM3BL
(240): Bind head tapping screw-B A3.0×6 FCM3BL

3. LCD Unit Removal

3-1. Remove the top cover. (see procedure 1)
3-2. Remove the front panel assembly. (see procedure 2)
3-3. Remove the two (2) screws marked (150), five (5) screws marked (120) and two (2) screws marked (130). (Fig. 2 and Fig. 3)
3-4. Remove the three (3) screws marked (70). (Fig. 2)
3-5. Remove the three (3) plastic rivets marked (90) and straighten the part of the sub panel indicated with the arrow in the figure, then remove the sub panel. (Fig. 4)
3-6. Take the LCD unit out from the AD1/4 circuit board.

4. AD4/4 Circuit Board Removal

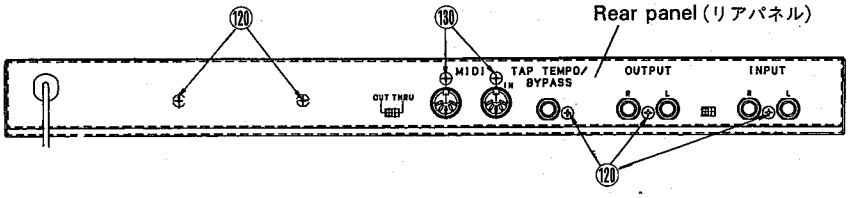
4-1. Remove the top cover. (see procedure 1)
4-2. Remove the front panel assembly. (see procedure 2)
4-3. Remove the two (2) screws marked (150), five (5) screws marked (120) and two (2) screws marked (130). (Fig. 2 and Fig. 3)
4-4. Remove the three (3) plastic rivets marked (90) and straighten the part of the sub panel indicated with the arrow in the figure, then remove the sub panel. (Fig. 4)
4-5. Take the AD4/4 circuit board out from the AD1/4 circuit board.

3．LCDユニットの外し方

3-1.トップカバーを外します。(1項参照)
3-2.フロントパネルAss'yを外します。(2項参照)
3-3.(150)のネジ2本を外し、リア側より(120)のネジ5本と(130)のネジ2本を外します。(図2、図3)
3-4.(70)のネジ3本を外します。(図2)
3-5.(90)のプラスチックリベット3個を外し、図中に矢印で示したサブパネルの金具をまっすぐにしてサブパネルを外します。(図4)
3-6.AD1/4シートからLCDユニットを外します。

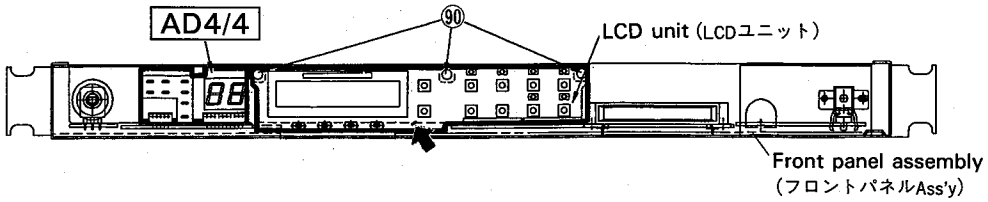
4．AD4/4シートの外し方

4-1.トップカバーを外します。(1項参照)
4-2.フロントパネルAss'yを外します。(2項参照)
4-3.(150)のネジ2本を外し、リア側より(120)のネジ5本と(130)のネジ2本を外します。(図2、図3)
4-4.(90)のプラスチックリベット3個を外し、図中に矢印で示したサブパネルの金具をまっすぐにしてサブパネルを外します。(図4)
4-5.AD1/4シートからAD4/4シートを外します。



(Fig. 3)

(120): Bind head tapping screw-B A3.0×6 FCM3BL
(130): Bind head tapping screw-B A3.0×8 FCM3BL



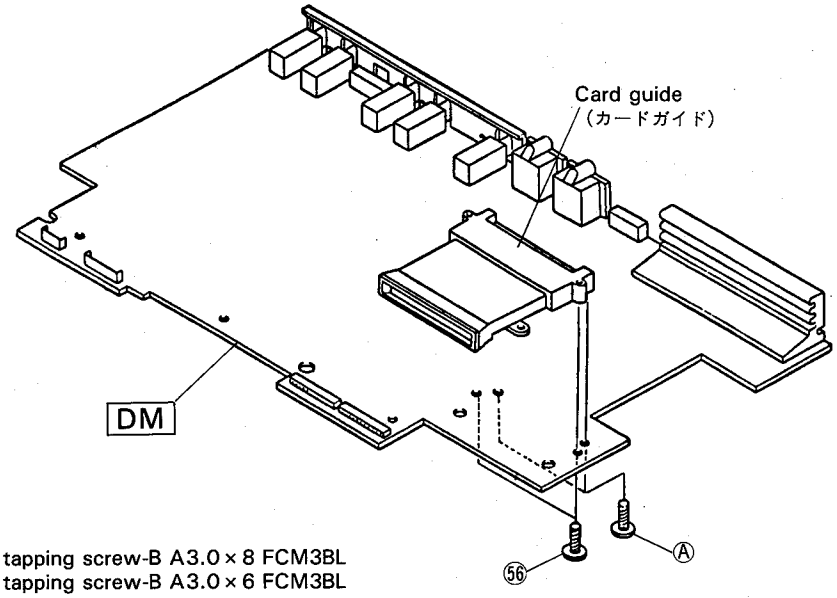
(Fig. 4)

5. AD1/4 Circuit Board Removal

5-1. Remove the top cover. (see procedure 1)
5-2. Remove the front panel assembly. (see procedure 2)
5-3. Remove the LCD unit. (see procedure 3)
5-4. Remove the AD4/4 circuit board. (see procedure 4)
5-5. Remove the two (2) screws marked (56) and two (2) screws marked (A), then remove the card guide. (Fig. 5)
* The card guide is not a part of the AD1/4 circuit board.

5．AD1/4シートの外し方

5-1.トップカバーを外します。(1項参照)
5-2.フロントパネルAss'yを外します。(2項参照)
5-3.LCDユニットを外します。(3項参照)
5-4.AD4/4シートを外します。(4項参照)
5-5.㊺のネジ2本とⒶのネジ2本を外し、カードガイドを外します。(図5)
(カードガイドはAD1/4シートの構成部品ではありません。)



(56) : Bind head tapping screw-B A3.0×8 FCM3BL
(A) : Bind head tapping screw-B A3.0×6 FCM3BL

(Fig. 5)

6. AD3/4 Circuit Board Removal

6-1. Remove the top cover. (see procedure 1)
6-2. Remove the front panel assembly. (see procedure 2)
6-3. Remove the two (2) level control knobs marked (250) and (260), and loosen the hexagonal nut marked (160), then remove the AD3/4 circuit board. (Fig. 6)

7. AD3/4 Circuit Board Removal (Power Switch Removal)

7-1. Remove the top cover. (see procedure 1)
7-2. Remove the front panel assembly. (see procedure 2)
7-3. Pull out the power switch knob.
7-4. After the screw marked (140) and two (2) screws marked (145) have been removed, then the AD2/4 circuit board can be removed. (Fig. 6)

8. Power Transformer Removal

8-1. Remove the top cover. (see procedure 1)
8-2. Remove the two (2) screws marked (180), then the power transformer can be removed. (Fig. 6)

6．AD3/4シートの外し方

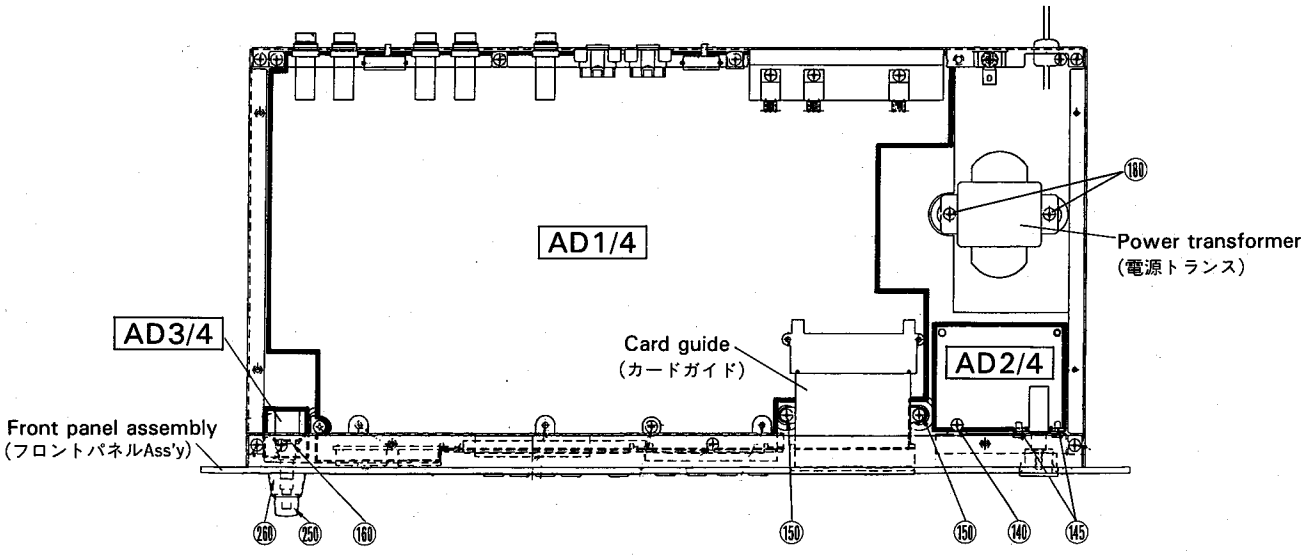
6-1. トップカバーを外します。(1項参照)
6-2. フロントパネルAss'yを外します。(2項参照)
6-3. (250)のVRツマミ（内）と(260)のVRツマミ（外）を外し、(160)の特殊六角ナットを緩めてAD3/4シートを外します。(図6)

7．AD2/4シート（パワースイッチ）の外し方

7-1. トップカバーを外します。(1項参照)
7-2. フロントパネルAss'yを外します。(2項参照)
7-3. パワースイッチツマミを外します。
7-4. (140)のネジ1本と(145)のネジ2本を外し、AD2/4シートを外します。(図6)

8．電源トランスの外し方

8-1. トップカバーを外します。(1項参照)
8-2. (180)のネジ2本を外し、電源トランスを外します。(図6)



(Fig. 6)

(140): Bind head tapping screw-B A3.0×6 FCM3BL
(145): Bind head screw A3.0×6 FCM3BL
(150): Bind head tapping screw-B A3.0×6 FCM3BL
(160): Hexagonal nut φ9.0 FCM3BL
(180): Bind head tapping screw-B 3.0×8 FCM3BL

■LSI PIN DESCRIPTION (LSI端子機能表)

• HD63B03YP-N (XD245A00) CPU (Central Processing Unit)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss		Ground	33	A17	O	Address bus
2	XTAL	I	Clock	34	A16	O	
3	EXTAL	I		35	A15	O	
4	MP0	I	Mode program	36	A14	O	
5	MP1	I		37	A13	O	
6	$\overline{RES}$	I	Reset	38	A11	O	
7	$\overline{STBY}$	I	Stand-by mode signal	39	A10	O	
8	$\overline{NMI}$	I	Non-maskable interrupt	40	A9	O	
9	P20	I/O	Port 2	41	A8	O	
10	P21	I/O		42	Vss		Ground
11	P22	I/O		43	A7	O	Address bus
12	P23	I/O		44	A6	O	
13	P24	I/O		45	A5	O	
14	P25	I/O		46	A4	O	
15	P26	I/O		47	A3	O	
16	P27	I/O		48	A2	O	
17	P50	I/O	Port 5	49	A1	O	
18	P51	I/O		50	A0	O	
19	P52	I/O		51	D7	I/O	Data bus
20	P53	I/O		52	D6	I/O	
21	P54	I/O		53	D5	I/O	
22	P55	I/O		54	D4	I/O	
23	P56	I/O		55	D3	I/O	
24	P57	I/O		56	D2	I/O	
25	P60	I/O	Port 6	57	D1	I/O	
26	P61	I/O		58	D0	I/O	
27	P62	I/O		59	$\overline{BA}$	O	Bus available
28	P63	I/O		60	$\overline{LIR}$	O	Load instruction register
29	P64	I/O		61	R/$\overline{W}$	O	Read/Write control
30	P65	I/O		62	$\overline{WR}$	O	Write control
31	P66	I/O		63	$\overline{RD}$	O	Read control
32	P67	I/O		64	E	O	Enable

• HD63B50P (IG147300) ACIA (Asynchronous Communications Interface Adaptor)

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	Vss		Ground	13	R/$\overline{W}$	I	Read/Write
2	Rx Data	I	Receive data	14	E	I	Enable
3	Rx CLK	I	Receive clock	15	D7	I/O	Data bus
4	Tx CLK	O	Transmit clock	16	D6	I/O	
5	$\overline{RTS}$	I/O	Request to send	17	D5	I/O	
6	Tx Data	O	Transmit data	18	D4	I/O	
7	$\overline{IRQ}$	I	Interrupt request	19	D3	I/O	
8	CS0	I	Chip select	20	D2	I/O	
9	$\overline{CS2}$	I		21	D1	I/O	
10	CS1	I		22	D0	I/O	
11	RS	I	Resist select	23	$\overline{DCD}$	I	Data carrier detect
12	Vcc		Power supply (+5V)	24	$\overline{CTS}$	I	Clear to send

• YSS208 (XI816A00) DSPN (Digital Signal Processor)

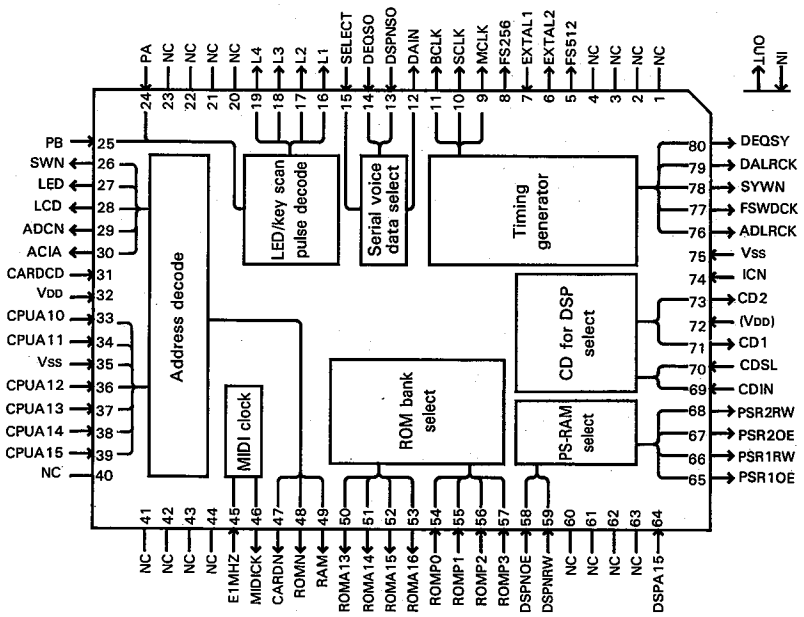
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	D9	I/O	External RAM data bus	33	A8	O	External RAM address bus
2	D8	I/O		34	A7	O	
3	D7	I/O		35	A6	O	
4	D6	I/O		36	A5	O	
5	D5	I/O		37	A4	O	
6	D4	I/O		38	A3	O	
7	D3	I/O		39	A2	O	
8	D2	I/O		40	A1	O	
9	D1	I/O		41	A0	O	
10	Vss		Ground	42	Vss		Ground
11	D0	I/O		43	TSTK	I	Test K
12	SI1	I	Data input	44	TST1	I	Test 1
13	SI0	I		45	CLKM	O	1/2 clock
14	SO1	O	Data output	46	SYW	I	Synch. signal input
15	SO0	O		47	CLK	I	Clock
16	XMD	I	ACIA synch. mode	48	CE	O	External RAM chip enable
17	XCLK	I	ACIA clock	49	IC	I	Initial clear
18	TO	O	Timer output	50	MDTST4	O	MOD data test
19	CRS	I	CDI reset	51	MDTST3	O	
20	CDO	O	Command output	52	MDTST2	O	
21	CDI	I	Command input	53	MDTST1	O	
22	TIM1	O	Timer 1	54	MDSI1	I	Wave add data input
23	OE	I	Output enable	55	MDSI0	I	
24	R/W	O	Read/write	56	MDSO2	O	Wave data output
25	A15	O	Power supply	57	MDSO1	O	
26	VDD			58	VDD		Power supply
27	A14	O	External RAM address bus	59	D15	I/O	External RAM data bus
28	A13	O		60	D14	I/O	
29	A12	O		61	D13	I/O	
30	A11	O		62	D12	I/O	
31	A10	O		63	D11	I/O	
32	A9	O		64	D10	I/O	

• PCM66P (XG278A00) DAC (Digital Analog Converter)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	L/R CK	I	LR Clock Input	11	+Vcc		+Vcc
2	WD CK	I	Word Clock Input	12	+Vcc		+Vcc
3	CK	I	Clock Input	13	C REF		Reference Decouple
4	DATA	I	Data Input	14	Vref Sense	I	Reference Sense
5	NC			15	Vref	O	Reference Output
6	DIG GND		Digital Ground	16	+Vcc		+Vcc
7	ANA GND		Analog Ground	17	+Vcc		+Vcc
8	L-CH OUT	O	Left Channel Output	18	+Vcc		+Vcc
9	V COM		V Common	19	M1	I	Mode 1 Input
10	R-CH OUT	O	Right Channel Output	20	M2	I	Mode 2 Input

• YSS218-F (XJ875A00) XLTM (Timing Generator/Address Decoder/Selector)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	NC			41	NC		
2	NC			42	NC		
3	NC			43	NC		
4	NC			44	NC		
5	FS512	O	Sampling freq. × 512	45	E1MHz	I	Clock, 1MHz
6	EXTAL1	I	Clock	46	M1DICK	O	MIDI clock, 500KHz
7	EXTAL2	O		47	CARDN	O	Card chip select
8	FS256	O	Sampling freq. × 256	48	ROMN	O	ROM chip select
9	MCLK	O	Sampling freq. × 128	49	RAM	O	RAM chip select
10	SCLK	O	Sampling freq. × 64	50	ROMA13	O	ROM address bus
11	BCLK	O	Sampling freq. × 64 ($\overline{SCLK}$)	51	ROMA14	O	
12	DAIN	O	Data output (DSPNSO or DEQSO)	52	ROMA15	O	
13	DSPNSO	I	Data input from DSPN	53	ROMA16	O	
14	DEQSO	I	Data input from DEQ	54	ROMP0	I	Bank select
15	SELECT	I	Input select (0: DSPNSO 1: DEQSO)	55	ROMP1	I	
16	L1	O	LED/key scan pulse	56	ROMP2	I	
17	L2	O		57	ROMP3	I	
18	L3	O		58	DSPNOE	I	DSP-RAM output enable
19	L4	O		59	DSPNRW	I	DSP-RAM write pulse
20	NC			60	NC		
21	NC			61	NC		
22	NC			62	NC		
23	NC			63	NC		
24	PA	I	LED/key scan input (bit 0)	64	DSPA15	I	DSP-RAM address bus
25	PB	I	LED/key scan input (bit 1)	65	PSR1OE	O	DSP-RAM1 output enable
26	SWN	O	Key data input enable	66	PSR1RW	O	DSP-RAM1 write pulse
27	LED	O	LED data enable	67	PSR2OE	O	DSP-RAM2 output enable
28	LCD	O	LCD data enable	68	PSR2RW	O	DSP-RAM2 write pulse
29	ADCN	O	ADC enable	69	CDIN	I	Control data input
30	ACIA	O	ACIA enable	70	CDS	I	Control data output select
31	CARDCD	I	RAM card detection	71	CD1	O	Control data output 1
32	VDD		Power supply	72	VDD		Power supply
33	CPUA10	I	CPU address bus	73	CD2	O	Control data output 2
34	CPUA11	I		74	ICN	I	Reset
35	Vss		(Ground)	75	Vss		Ground
36	CPUA12	I		76	ADLRCK	O	ADC data select (1: L 0: R)
37	CPUA13	I		77	FSWDCK	O	Sampling freq. × 2
38	CPUA14	I		78	SYWN	O	Synch. signal
39	CPUA15	I		79	DALRCK	O	DAC data L/R latch signal
40	NC			80	DEQSY	O	Synch. signal for DEQ



• **YM6104** (XE788A00) DEQ2 (Digital Equalizer)

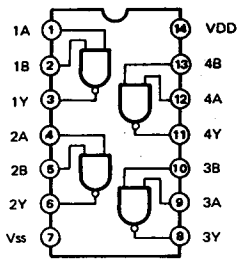
Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	VDD	I	+5V	12	Vss	I	Earth (Ground)
2	XHD	I	Alteration of Sync. (=+5V) or Asynch. (=0V) for CDI input terminal (Synch: 1:1), Asynch: 16:1)	13, 14	SI0, SI1	I	INPUT for Serial data signal
				15, 16	SO0, SO1	O	OUTPUT for Serial data signal
				17	$\overline{OVF}$	O	Detector for OVER Flow
3	$\overline{CRS}$	I	Initialized Serial Control Interface	18	$\overline{TEST}$	I	For test. Normally connecting to +5V
4	CDI	I	Inputs of μ PGM, Para, Ser. Cont. Data of Control Reg.	19	C2	O	Output is delayed Data of 2nd bit of P. Reg. by 1 bit.
5	CDO	O	Outputs of μ PGM, Para, Ser Cont. Data of Control Reg.	20	C1	O	Output is delayed Data of 1st bit of P. Reg. by 1 bit.
6	XCLK	I	In/Out clock for CDI & CDO	21	C0	O	Output is delayed Data of 0 bit of P. Reg. by 1 bit.
7	TRG	I	Determins transmit timming of PARA. to Para. Reg. from T BFR.	22	CEMD	I	+5V: It's necessory to input 2 Byte for CE to CDI
8	ESL	I	Timming determination of data for External at Ext. Shift CLK				0V: It needs not to have a data for CE to CDI
9	ELD	I	Timming determination of data for Inner at Ext. Shift CLK	23	$\overline{IC}$	I	Initialized for DEQ
10	ECLK	I	Input Shift CLK of IN/OUT SR at Ext Shift CLK	24	$\overline{SYW}$	I	Synchro. signal for system
11	CLK	I	System Clock				

• **AK5339-VP** (XI112A00) DAC (Digital Analog Converter)

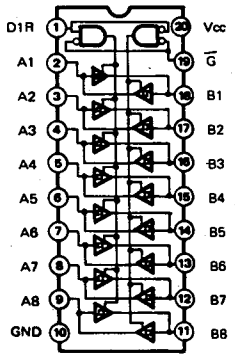
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	AGND		Analog ground	15	SCLK	I	Serial output data clock
2	AINL	I	Left channel analog input	16	SDATA	O	Serial data output
3	ZEROL	I	Zero level input for left channel	17	FSYNC	I	FSYNC signal input
4	VA+		Positive analog power supply	18	VD+		Positive digital power supply
5	VA−		Negative analog power supply	19	DGND		Digital ground
6	APD	I	Analog power down	20	CLK	I	Digital section input clock
7	ACAL	I	Analog calibrate	21	OCLK	O	Clock output
8	NC		No connection	22	NC		NC
9	DCAL	O	Digital calibrate output	23	CLKIN	I	Master input clock
10	DPD	I	Digital power down	24	LGND		Logic ground
11	TST	I	Test inputs	25	VL+		Positive logic power supply
12	CMODE	I		26	ZEROR	I	Zero level input for right channel
13	SMODE	I		27	AINR	I	Right channel analog input
14	L/$\overline{R}$	I	Left/Right select	28	VREF	O	Voltage reference output

■ IC BLOCK DIAGRAM (ICブロック図)

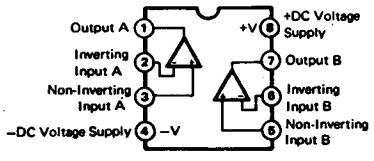
• **TC74HC00AP** (IR000000)
• **SN74HC00N** (IR000050)
Quad 2 Input NAND



• **TC74HC245AP** (IR024500)
Octal 3-State Bus Transceiver



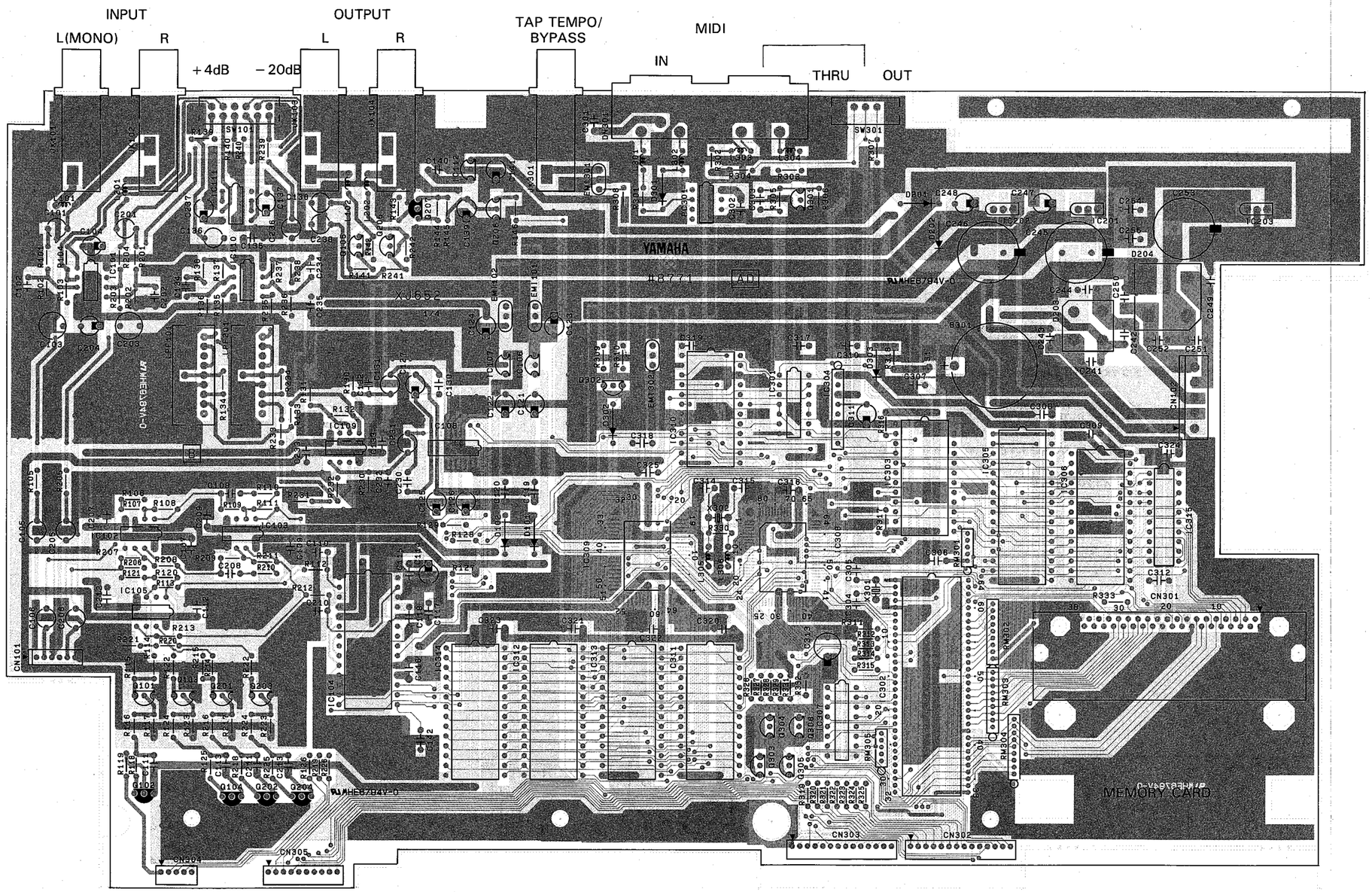
• **RC4558D-V** (IG001390)
Dual Operational Amplifier



EMP700

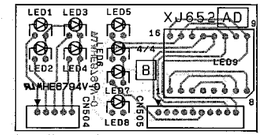
■ CIRCUIT BOARD（シート基板図）

● AD1/4 Circuit Board



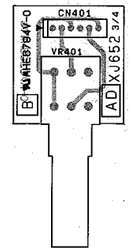
Components side（部品側）

● AD2/4 Circuit Board



Components side（部品側）

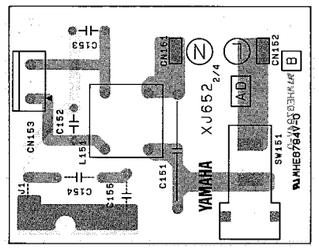
● AD3/4 Circuit Board



INPUT LEVEL
(L/R)

Components side（部品側）

● AD4/4 Circuit Board



POWER

Components side（部品側）

Notes)

Circuit Board: AD (VL379000) XJ652A0 J,U,C,V
AD (VL379100) XJ652A0 H,B

1. IC
IC101～103, 105,109～111: RC4558D-V (IG001390) OP AMP.
IC104: AK5339-VP (XI112A00) ADC
IC106: μPC78L05J (XC349A00) 5V REGULATOR
IC107: NJM79L05A (IG130500) －5V REGULATOR
IC108: PCM66P (XG278A00) DAC
IC112: NJM78L12A (XD066A00) 12V REGULATOR
IC201: NJM7812FA (XC720A00) 12V REGULATOR
IC202: NJM7912FA (XC721A00) －12V REGULATOR
IC203: NJM7805FA (XC719A00) 5V REGULATOR
IC301: TC74HC00AP (IR000000) NAND or SN74HC00N (IR000050) NAND
IC302: HD63B03YP-N (XD245A00) CPU
IC303: HD63B50P (IG147300) ACIA
IC304: M62021L (XH970A00) RESET
IC305: (XK356A00) 1M EPROM
IC306: LC3664RL-12 (XG517A00) SRAM 64K
IC308: YSS218-F (XJ875A00) XLTM
IC309: YSS208 (XI816A00) DSPN
IC310: YM6104 (XE788A00) DEQ2
IC311～314: TC51832PL-10 (XC628A00) PSRAM 256K or HM65256BLP-10 (XH116A00) PSRAM 256K
IC315: TC74HC245AP (IR024500) BUS BUFFER

2. Photo Coupler
PC301: 6N137 (VD473200)

3. Transistor
Q101,103,201, 203,301,302: 2SC1815 Y (IC1815I0)
Q102,104, 202,204,207: 2SA1015 Y (IA1015I0)
Q105,205,206: 2SC2878 B (VC710400)
Q303～306: 2SC1213A D (IC121340)

4. Transistor Array
IC307: TD62506P (IG138700)

5. Diode
D101,102,201,202: 11ES4 (VB481900)
D301～303: 1SS133,1SS176 (VB941200)

6. Diode Stack
D203: S2VB20 2A 200V (IH001120)
D204: 4D4B41 4A 200V (IH000870)

7. LED
LED 1,3,8: GL8HD26 RE (VK018900) PEAK(L,R),MIDI
LED 2,4～7: GL8KG26 GR (VJ734900) SIGNAL(L,R),PRESET, USER,CARD

8. LED Display
LED 9: LN524RKS (VA026000)

9. Resistor Array
RM301,305: RGLE4X103J (VF773500)
RM302～304: RGLE8X103J (VF771900)

10. Variable Resistor
VR401: A10K × 2 RK124222 (VL962700) INPUT LEVEL(L,R)

11. Electrolytic Cap.
C245,246: 2200μF 25V (UJ749220)
C253: 2200μF 16V (UJ739220)

12. Ceramic Cap.
C151: 0.1μF (FR203100)
C152,153: 2200pF 400V (FI383220)
C154,155: 4700pF 400V (FI383470) H,B

13. Semiconductive Cera. Cap.
0.1μF 25V Z (VC694800)

14. Coil
L101,102,201, 202,301～304: FL5R200QNT (VB835000) 20μH
L151: PLA3021A 3mm (GD900760)

15. LC Filter
LPF101,201: LPF 20KHZ (VH408900)

16. EMI Filter
EMI101,102, 301,302: LS MT Y223NB (FZ006970)

17. Ferrite Bead
L305,306: BL02RN1-R62T4 (GE300610)

18. Ceramic Resonator
X301: 4MHz CSA4.00MG (QU004800)
X302: CSA22.5792MG (VH409300)

19. Thermistor
R332: ERT-D2FK103S1K (VN140900)

20. Push Switch
SW151: ESB-82TYPE (VJ557300) POWER SWITCH

21. Slide Switch
SW101: SSSU142-S06S-0 (VM475900) －20dB,＋4dB
SW301: SSSU112-S06S-0 (VM476100) MIDI OUT/THRU

22. DIN Jack
DN301: 5P3 YKF51-50 (VK519000) MIDI(IN,OUT/THRU)

23. Phone Jack
JK101～104,301: YKB21-5012 (VB312600) INPUT(L,R), OUTPUT(L,R),TAP TEMPO/BYPASS

24. Connector, Card
CN301: IC3A38PS-1.27D 38P (VF821100) MEMORY CARD

25. Lithium Battery
B301: SONY/CR2032 (VE338400)

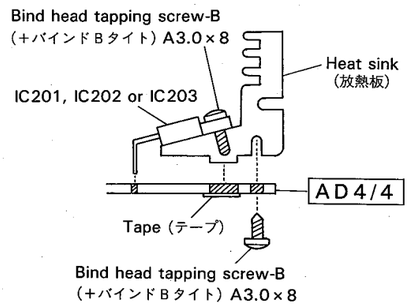
26. Terminal
CN151,152: (VA855400)

27.

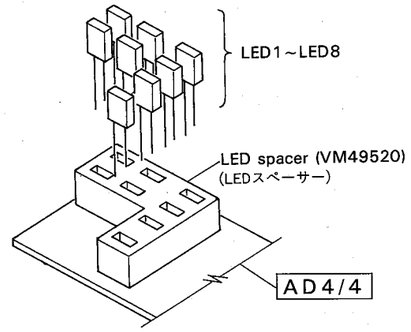
	J1	C154	C155
VL379000 (J,U,C,V)	○	×	×
VL379100 (H,B)	×	○	○

(○: installed ×: not installed)

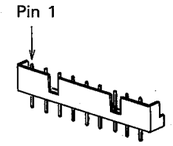
• IC201, IC202 and IC203 installation
(IC201～IC203の取り付け)



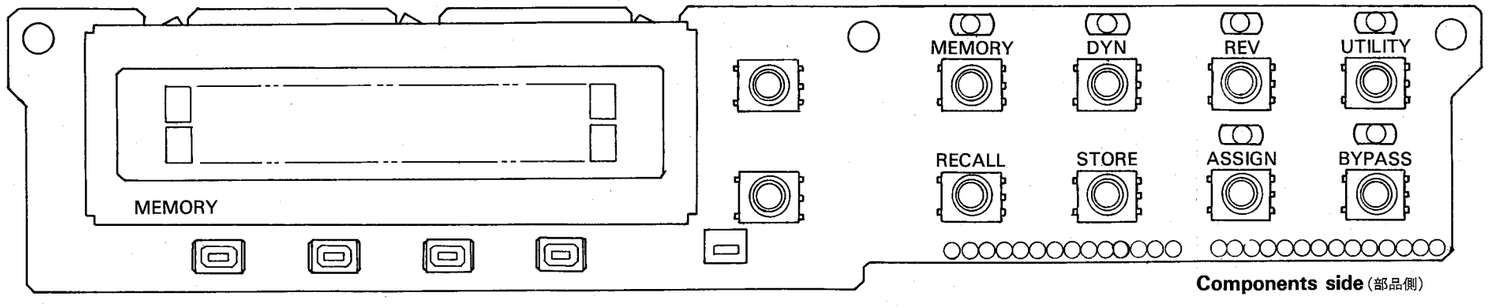
• LED1～LED8 installation
(LED1～LED8の取り付け)

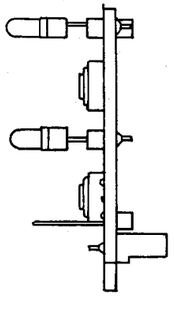


• CN304 and CN305



• LCD UNIT





Notes)

LCD Unit: (VL842500)

1. IC
IC1: NJU64720-02

2. LED
LED 1～6: TLR220 RE (VE464300)

3. LED Back-lit
LED 7:

4. Tact Switch
SW 1～10: SKHUQB
SW11～14: SKHLAC023A (VC021100)

■ TEST PROGRAM

A. HOW TO ENTER THE TEST PROGRAM

While pressing the [Function 1] key and [DYN] key, turn on the power switch.

B. PROCEEDING THROUGH THE TESTS

When you have entered the test program, select a test number by using the ▲ and ▼ keys, and then press the [RECALL] key to execute the test.

C. EXIT TEST PROGRAM

To exit the test program mode and return to normal operation, select the test number "50", then press the [RECALL] key. Activating the test 7 after performing tests 1 through 5 will restore normal operation too.

If the test 7 is executed without completion of tests 1 through 6, "CHECK NOT END" message will appear on the LCD, and the test that are performed will be shown by following LED switch indicators:

TEST 1: [MEMORY]
TEST 2: [DYN]
TEST 3: [REV]
TEST 4: [UTILITY]
TEST 5: [ASSIGN]
TEST 6: [BYPASS]

C. INITIAL TEST

After the system has entered the test program, the ACIA check will be performed automatically and a signal passes through the digital effect circuit. When the test checks OK, the LCD display will indicate "TEST ACIA. OK".

(The SRAM check is performed automatically when the power is applied to the unit on normal operation.)

TEST 1. LCD TEST

Check that all dots of the LCD turn ON and OFF five times, then the TEST END message will appear on the LCD.

```
DIAGNOSIS V1.0
TEST LCD    END
```

TEST 2. LED ON/OFF TEST

Check that each LED blinks once in succession from the left end of the unit.

First, check that 7-segment LED will display in sequence numbers "00" through "99", then the PRESET, USER, CARD and MIDI LED indicators blink one after another, and each switch LED blinks once in succession.

Next, verify all LEDs light and then turn off together, finally, 7-segment LED will show "2". The LEVEL indicators will remain OFF during this test.

TEST 3. PANEL AND FOOT SWITCH TEST

Press the panel switches consecutively from the [Function 1] switch to foot switch [TAP TEMPO/ BYPASS], according to the order indicated by the LCD.

```
DIAGNOSIS V1.0
TEST SWITCH F1
```

(e.g. When checking [Function 1].)

If the switch is OK, you should proceed to the next switch. If the wrong switch is pressed, the error message NG will be displayed. At this time, press the [RECALL] key to initiate this test.

```
DIAGNOSIS V1.0
TEST SWITCH NG
```

When the switch name "TAP" is displayed on the LCD, attach a foot switch to the TAP TEMPO/ BYPASS jack on the rear panel, then press it to check. If checks OK, 'OK' is displayed on the LCD and the test will end.

```
DIAGNOSIS V1.0
TEST SWITCH OK
```

TEST 4. MEMORY CARD TEST

This test performs a read/write test on the RAM card, a card insert test and a write protect switch test. Insert a RAM card with the memory protect switch turned off and execute the test.

DISPLAY OF TEST RESULTS

OK

```
DIAGNOSIS V1.0
TEST CARD  R/W
```

NG

```
DIAGNOSIS V1.0
TEST CARD   NG
```

Then check that when you remove the card, the message on the display will be as follow:

```
DIAGNOSIS V1.0
TEST CARD  NON
```

Next, check that when the memory protect switch is set from "protect off" to "protect on" and insert the card back into the slot, the display will show the following message.

```
DIAGNOSIS V1.0
TEST CARD  PRO
```

TEST 5. MIDI TEST
After connecting the MIDI IN to the MIDI OUT via a MIDI cable, execute the test. The test results will be displayed on the LCD.

```
DIAGNOSIS V1.0
TEST MIDI   OK
```
(e.g. When the test is OK.)

```
DIAGNOSIS V1.0
TEST MIDI   NG
```
(e.g. When unexpected data was received.)

```
DIAGNOSIS V1.0
TEST MIDI   NG
```
(e.g. When no data was received.)

TEST 6. FACTORY SET TEST
This test is used to initialize the data to the factory settings.
When this test is executed, the following display will appear.

```
DIAGNOSIS V1.0
RAM INITIALIZE?
```

If you press the [STORE] key, the factory preset data will be restored, the LCD will display the message shown below.

```
DIAGNOSIS V1.0
RAM INITIALIZE
```

TEST 7. DEQ2 CHIP TEST
Check that a correct sine wave of 880Hz, 12dBm is output using an oscilloscope.

```
DIAGNOSIS V1.0
TEST DEQ2
```

TEST 8. DSPN CHIP TEST
Check that a correct sine wave of 880Hz, 12dBm is output using an oscilloscope.

```
DIAGNOSIS V1.0
TEST DSPN
```

■ INITIALIZATION

While pressing the [Function 1] key and [▲] key, turn on the power switch, then the RAM data will be initialized and other parameters are set with the factory setting data.

■ INSPECTIONS

Before performing any following adjustments, set the unit as follows:
1. Input level controls: maximum
2. Set the −20dB/+4dB switch at +4dB
3. Short the L and R outputs with 10kohm loads.
4. BYPASS switch: ON

1. Gain test

Check that the OUTPUT should be −10dBm± 1.5dB, when a sine wave of 100Hz at −20dBm is applied to the INPUT L.
When the −20dB/+4dB switch is turn to −20dB, the OUTPUT level should also be −10dBm±1.5dB.

2. Frequency response test

When a sine wave of 0dBm is applied to the INPUT L, check that the output is as follows. (taking 1kHz as a reference)

20Hz~5kHz	±1.5dB
6kHz~18kHz	±1.5dB
24kHz	less than −10dB

3. Residual noise test

When the input is opened, residual noise should be less than −67dBm.
(Use a 12.7kHz, −6dB/oct. filter)

4. Maximum output level, distortion factor and channel separation test

Check that the output is +17dBm when a sine wave of 1kHz is applied, and when the input level is adjusted, making the distortion rate less than 0.03%.
Then increase the input level to obtain the output of +18dBm, check that the distortion rate is less than 0.1%.
Next, Apply no signal to the INPUT L, check that the L OUTPUT level should be less than −50 dBm.
(Check the R channel in same manner.)

5. Measuring instruments

1. For the distortion measurement, a low-pass filter with cut-off frequency of 80kHz, −6dB/oct. must be used.
2. For the noise level measurement, a low-pass filter with cut-off frequency of 12.7kHz, −6dB/oct. must be used.
3. The output impedance of the signal generator must be less than 600ohms.
4. The input impedance of the measuring instruments must be over 1Mohms.

■テストプログラム

テストプログラムの起動

[F1]と[DYN]キーを押しながら、電源スイッチをONします。

テストプログラムの進め方

[▲]と[▼]キーを使用して実行するテスト番号を選択した後、[RECALL]キーを押してテストを実行します。

テストの終了の仕方

テスト50を実行すると、テストプログラムモードを抜けて通常モードとなります。また、テスト1からテスト5までを全て終了した後にテスト7を実施しても、テストプログラムを終えることができます。テスト1からテスト5までを終了せずにテスト7を実施すると、"CHECK NOT END"がLCDに表示されると共に、以下に示すスイッチのLEDが点灯し、終了したテストを示します。

テスト1：[MEMORY] LED
テスト2：[DYN] LED
テスト3：[REV] LED
テスト4：[UTILITY] LED
テスト5：[ASSIGN] LED
テスト6：[BYPASS] LED

A．イニシャルテスト

テストプログラムが起動されると、LSIの回線チェックが実行されます。
テストがOKなら、"TEST ACIA. OK"がLCDに表示されます。
(SRAMチェックは、通常動作時の電源スイッチONのときに、実行されます。)
なお、テストプログラムが起動されると、AD/DA回路はダイレクト信号のみをOUTPUT LとRに出力します。

テスト1　LCD表示器の動作チェック

テストが起動されると、LCDの全ドットが5回点滅し、その後、次の画面が表示されます。

```
DIAGNOSIS V1.0
TEST LCD    END
```

テスト2　LEDの点灯チェック

LEDが全て点灯するか、目視によりチェックします。

1．メモリーLEDが、"00"、"11"、"22"と順次点灯します。
2．[PRESET]、[USER]、[CARD]、[MIDI]のLEDが、順次点灯します。
3．スイッチ上のLEDが、1個ずつ順次点灯します。
4．全LEDが点灯します。(レベルメーター用のLEDは除く)
5．LEDが消灯し、メモリーLEDが"2"を表示して停止します。

テスト3　スイッチの動作確認

テストが起動されると、次の画面がLCDに表示されます。

```
DIAGNOSIS V1.0
TEST SWITCH F1
```

(F1の部分は、点滅している)

1．[F1]キーを押すと、[F1]のブリンクが[F2]に変わります。
2．[F2]キーを押すと、[F2]のブリンクが[F3]に変わります。
以下、LCDの表示に従ってスイッチを順番に押していきます。
3．[BYPASS]キーを押すと、[TAP]のブリンクに変わります。そうしたら、[TAP TEMPO/BYPASS]のフットスイッチ用ジャックにフットスイッチを接続し、ONします。
テストがOKなら、次の画面がLCDに表示されます。

```
DIAGNOSIS V1.0
TEST SWITCH OK
```

スイッチを押し間違えたときは、テストを再起動してやり直して下さい。

テスト 4　メモリーカードのI/Oポートのチェック

メモリーカードのライトプロテクトスイッチをOFFにして、テストを起動します。

カードに書き込み、読み出しができた場合

```
DIAGNOSIS V1.0
TEST CARD  R/W
```

カードに書き込み、読み出しができなかった場合

```
DIAGNOSIS V1.0
TEST CARD   NG
```

次に、メモリーカードをスロットから抜きます。これを確認できたときは、次のように表示されます。

```
DIAGNOSIS V1.0
TEST CARD  NON
```

さらに、メモリーカードのライトプロテクトスイッチをONにして、もう一度差し込みます。これを確認できた場合は、次のように表示されます。

```
DIAGNOSIS V1.0
TEST CARD  PRO
```

手順を間違えたときは"NG"となるので、テストを再起動してやり直して下さい。

テスト 5　MIDIの入出力チェック

MIDI INとMIDI OUTをMIDIケーブルで接続した後、テストを起動します。

テストがOKのとき

```
DIAGNOSIS V1.0
TEST MIDI   OK
```

MIDI OUTから出力された信号がMIDI INを経由してCPUに戻ってこないとき

```
DIAGNOSIS V1.0
TEST MIDI   NG
```

信号は戻ってくるが、正常でないとき

```
DIAGNOSIS V1.0
TEST MIDI   NG
```

テスト 6　ユーザーRAMの初期設定

テストが起動されると、次の画面が表示されます。

```
DIAGNOSIS V1.0
RAM INITIALIZE?
```

[STORE] キーを押すと、ユーザーRAM領域にファクトリープリセット値がセットされると共に、各パラメータ値も初期値に設定され、LCD画面は次のように変わります。

```
DIAGNOSIS V1.0
RAM INITIALIZE
```

テスト 7　DEQ2-LSIのチェック

テストが起動されるとDEQ2から約880Hz、12dBmの正弦波が出力されるので、これをオシロスコープで観測してLSIが正常かどうか判断します。テスト中は、次の画面が表示されます。

```
DIAGNOSIS V1.0
TEST DEQ2
```

テスト 8　DSPN-LSIのチェック

テストが起動されるとDSPNから約880Hz、12dBmの正弦波が出力されるので、これをオシロスコープで観測してLSIが正常かどうか判断します。テスト中は、次の画面が表示されます。

```
DIAGNOSIS V1.0
TEST DSPN
```

■RAMのイニシャライズ

[F1] と [▲] キーを押しながら電源スイッチをONすると、RAMのデータはイニシャライズされ、その他のパラメータも初期値に設定されます。

■検査

・準備

特に指定のない限り、パネルのボリュームおよびスイッチは、下記の状態とする。

1．INPUTレベルコントロール(L、R)　：最大
2．＋4dB/－20dBスイッチ　：＋4ｄＢ
3．BYPASSキー　：ＯＮ
4．OUTPUT(L、R)端子に10kΩの負荷を接続する

1．利得

INPUT(L)より100Hz/－20dBmの信号を加えたとき、＋4dB/－20dBスイッチがいずれの側に設定されていても、OUTPUT(L、R)端子には－10dBm±1.5dBの出力が得られること。

2．周波数特性

INPUT(L)より0dBm程度の信号を加えたとき、OUTPUT(L、R)端子の出力信号の周波数特性は、1kHzを基準として下表の範囲にあること。

20Hz－5kHz	±1.5dB
6kHz－ 18kHz	±1.5dB
24kHz	－10dB以下

3．ノイズレベル

INPUT端子に接続されているプラグを抜いたとき、OUTPUT(L、R)端子でのノイズレベルは－67dBm以下のこと。(12.7kHz、－6dB/octのフィルターを使用すること)

4．最大出力、歪率、チャンネルセパレーション

INPUT(L、R)端子それぞれに1kHzの信号を入力します。入力信号のレベルを徐々に大きくしていったとき、OUTPUT(L、R)端子には＋17dBmの出力が歪率0.03%以内で得られること。また、出力が＋18dBmのときの歪率は1%以内のこと。

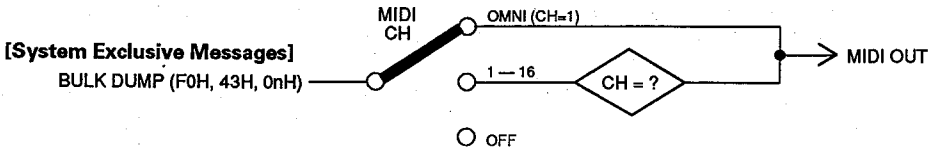
このとき、INPUT(L)端子に加えられている信号をOFFすると、OUTPUT(L)端子の出力信号レベルは－50dBm以下のこと。次に、INPUT(L)端子にもう一度信号を加えた後、INPUT(R)端子に加えられている信号をOFFすると、OUTPUT(R)端子の出力信号レベルは－50dBm以下のこと。

4　測定器

1　歪率測定時は、80kHz、－6dB/octのフィルターを使用すること。
2　ノイズレベル測定時は、12.7kHz、－6dB/octのフィルターを使用すること。
3　発信器の出力インピーダンスは、600Ω以下のこと。
4　測定器の入力インピーダンスは、1MΩ以上のこと。

■ MIDI DATA FORMAT

1. TRANSMISSION CONDITIONS



2. TRANSMISSION DATA

2-1. System Information

[1] System Exclusive Messages

- **BULK DUMP**

  Bulk dump messages can be transmitted when the MIDI OUT/THRU select switch of the EMP700 is set to the "OUT" position.

  The combination of bulk dump data to be transmitted can be selected in the utility mode.

1) 1 MEMORY BULK DATA

When a 1 MEMORY BULK OUT operation is performed or when a 1 MEMORY BULK DUMP REQUEST message is received by the EMP700, the data is transmitted on the MIDI channel specified for the currently selected BANK.

STATUS	11110000(F0H)	SYSTEM EXCLUSIVE
ID NO.	01000011(43H)	YAMAHA
SUB STATUS	0000nnnn	nnnn = CHANNEL NO. *1
FORMAT NO.	01111110(7EH)	UNIVERSAL BULK DUMP
BYTE COUNT	00000001(01H)	HEADER & DATA = 168 bytes
	00101000(28H)	
HEADER	01001100(4CH)	"L"
	01001101(4DH)	"M"
	00100000(20H)	" "
	00100000(20H)	" "
	00111000(38H)	"8"
	00110111(37H)	"7"
	00110111(37H)	"7"
	00110001(31H)	"1"
DATA NAME	01001101(4DH)	"M"(1 MEMORY DATA)
MEMORY NO.	0mmmmmmm	mmmmmmm = USER MEMORY NO. *8
DATA	0000dddd	1st byte *9
	:	:
	:	:
	0000dddd	160th byte
CHECKSUM	0eeeeeee	*10
EOX	11110111(F7H)	

2) 1 BANK PROGRAM CHANGE TABLE BULK DATA

When a 1 BANK PROGRAM CHANGE TABLE BULK OUT operation is performed or when a 1 BANK PROGRAM CHANGE TABLE BULK DUMP REQUEST message is received by the EMP700, the data is transmitted on the MIDI channel specified for the currently selected BANK.

STATUS	11110000(F0H)	SYSTEM EXCLUSIVE
ID NO.	01000011(43H)	YAMAHA
SUB STATUS	0000nnnn	nnnn = CHANNEL NO. *1
FORMAT NO.	01111110(7EH)	UNIVERSAL BULK DUMP
BYTE COUNT	00000010(02H)	HEADER & DATA = 266 bytes
	00001010(0AH)	
HEADER	01001100(4CH)	"L"
	01001101(4DH)	"M"
	00100000(20H)	" "
	00100000(20H)	" "
	00111000(38H)	"8"
	00110111(37H)	"7"
	00110111(37H)	"7"
	00110001(31H)	"1"
DATA NAME	01010100(54H)	"T"(1BANK DATA)
BANK NO.	00000bbb	bbb = BANK NO. *11
DATA	00000bbb	1st byte *12
	:	:
	:	:
	00000bbb	256th byte
CHECKSUM	0eeeeeee	*10
EOX	11110111(F7H)	

3) SYSTEM SETUP BULK DATA

When a SYSTEM SETUP BULK OUT operation is performed or when a SYSTEM SETUP BULK DUMP REQUEST message is received by the EMP700, the data is transmitted on the MIDI channel specified for the currently selected BANK.

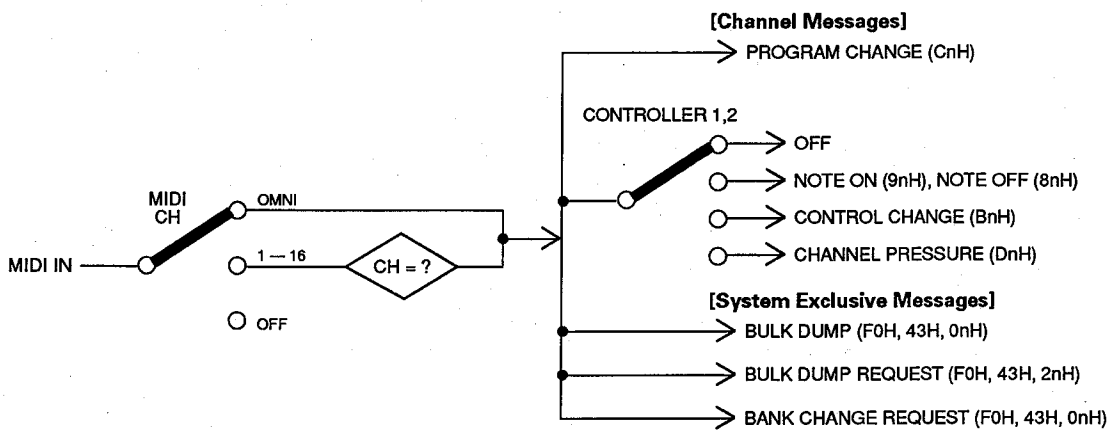
STATUS	11110000(F0H)	SYSTEM EXCLUSIVE
ID NO.	01000011(43H)	YAMAHA
SUB STATUS	0000nnnn	nnnn = CHANNEL NO. *1
FORMAT NO.	01111110(7EH)	UNIVERSAL BULK DUMP
BYTE COUNT	00000000(00H)	HEADER & DATA = 20 bytes
	00010100(14H)	
HEADER	01001100(4CH)	"L"
	01001101(4DH)	"M"
	00100000(20H)	" "
	00100000(20H)	" "
	00111000(38H)	"8"
	00110111(37H)	"7"
	00110111(37H)	"7"
	00110001(31H)	"1"
DATA NAME	01010011(53H)	"S"(SYSTEM SETUP DATA)
	00100000(20H)	" "
VERSION NO.	0vvvvvvv	VERSION NO. MSB
	0vvvvvvv	VERSION NO. LSB
CHANNEL NO.	000nnnnn	bank A *13
	000nnnnn	bank B
	000nnnnn	bank C
	000nnnnn	bank D
BANK NO.	000000bb	CURRENTLY SELECTED BANK NO. *11
CONTROL NO.	0ccccccc	CONTROLLER 1 *14
	0ccccccc	CONTROLLER 2
FOOTSWITCH	0000dddd	FOOTSWITCH ASSIGNMENT *15
CHECKSUM	0eeeeeee	*10
EOX	11110111(F7H)	

4) ALL BULK DATA

When an ALL BULK OUT operation is performed or when an ALL BULK DUMP REQUEST message is received by the EMP700, the data is transmitted on the MIDI channel specified for the currently selected BANK.

All user program data from U01 to U50, all bank program change tables A through D, and system setup data will be transmitted in this order and in the formats described in (1) to (3) above.

3. RECEPTION CONDITIONS



4. RECEPTION DATA

4-1. Channel Information

[1] Channel Voice Messages

1) NOTE ON

Received on the channel specified for the selected bank when a program with controllers 1 and 2 assigned to KEY NOTE or KEY VEL. is active or when a pitch change meter effect (TPI, SPI, P+R, P→R) and a parameter setting other than OFF are selected.

When a message is received, the value of the assigned effect parameter is changed according to the note number or velocity value or the pitch change course value changes according to the note number.

```
STATUS      1001nnnn(9nH)  nnnn = Channel No. *1
1st data    0kkkkkkk       kkkkkkk = Note No. *2
2nd data    0vvvvvvv       vvvvvvv = Velocity  *3
```

2) NOTE OFF

This message affects the EMP700 only when the equipment signalling the end of a NOTE ON message is connected.

```
STATUS      1000nnnn(8nH)  nnnn = Channel No. *1
1st data    0kkkkkkk       kkkkkkk = Note No. *2
2nd data    0vvvvvvv       vvvvvvv = Velocity *3
```

3) CONTROL CHANGE

Received on the channel specified for the selected bank when a program with controllers 1 and 2 assigned to either 01 (MOD. WHEEL) ~ 31 or 64 (SUSTAIN) ~ 95 is active.

When a message is received, the value of the assigned effect parameter is changed according to the control value.

```
STATUS      1011nnnn(BnH)  nnnn = Channel No. *1
1st data    0ccccccc       ccccccc = Control No. *4
2nd data    0vvvvvvv       vvvvvvv = Control Value *5
```

4) PROGRAM CHANGE

Received on the MIDI channel specified for the currently selected bank.

When a message is received, the corresponding program is called from the program change table of the selected bank.

```
STATUS      1100nnnn(CnH)  nnnn = Channel No. *1
1st data    0ppppppp       ppppppp = Program No. *6
```

5) CHANNEL PRESSURE

Received on the channel specified for the selected bank when a program with controllers 1 and 2 assigned to CH PRES. in the UTILITY mode is active.

When a message is received, the value of the assigned parameter is changed according to the pressure value.

```
STATUS      1101nnnn(DnH)  nnnn = Channel No. *1
1st data    0vvvvvvv       vvvvvvv = Pressure Value *7
```

4-2. System Information

[1] System Exclusive Messages

1) 1 MEMORY BULK DATA

Received on the MIDI channel specified for the currently selected bank.
When received, the currently active program data is erased and replaced by the received data.
The data format is the same as for transmission.

2) 1 BANK PROGRAM CHANGE TABLE BULK DATA

Received on the MIDI channel specified for the currently selected bank.
When received, the currently active program change table is erased and replaced by the received data.
The data format is the same as for transmission.

3) SYSTEM SETUP BULK DATA

Received on the MIDI channel specified for the currently selected bank.
When received, the currently active system setup data is erased and replaced by the received data.
The data format is the same as for transmission.

4) ALL BULK DATA

Received on the MIDI channel specified for the currently selected bank.
When received, virtually all currently active data is erased and replaced by the received data.
The data format is the same as for transmission.

5) 1 MEMORY BULK DUMP REQUEST

Received on the MIDI channel specified for the currently selected bank.
When received, the data corresponding to the specified USER program is transmitted.

STATUS	11110000(F0H)	SYSTEM EXCLUSIVE
ID NO.	01000011(43H)	YAMAHA
SUB STATUS	0010nnnn	nnnn = CHANNEL NO. *1
FORMAT NO.	01111110(7EH)	UNIVERSAL BULK DUMP
BYTE COUNT	00000010(02H)	HEADER & DATA = 266 bytes
	00001010(0AH)	
HEADER	01001100(4CH)	"L"
	01001101(4DH)	"M"
	00100000(20H)	" "
	00100000(20H)	" "
	00111000(38H)	"8"
	00110111(37H)	"7"
	00110111(37H)	"7"
	00110001(31H)	"1"
DATA NAME	01001101(4DH)	"M"(1 MEMORY DATA)
DATA	0mmmmmmm	mmmmmmm = USER'S MEMORY NO.*8
EOX	11110111(F7H)	

6) 1 BANK PROGRAM CHANGE TABLE BULK DUMP REQUEST

Received on the MIDI channel specified for the currently selected bank.
When received, the data corresponding to the program change table of the specified bank is transmitted.

STATUS	11110000(F0H)	SYSTEM EXCLUSIVE
ID NO.	01000011(43H)	YAMAHA
SUB STATUS	0010nnnn	nnnn = CHANNEL NO. *1
FORMAT NO.	01111110(7EH)	UNIVERSAL BULK DUMP
BYTE COUNT	00000010(02H)	HEADER & DATA = 266 bytes
	00001010(0AH)	
HEADER	01001100(4CH)	"L"
	01001101(4DH)	"M"
	00100000(20H)	" "
	00100000(20H)	" "
	00111000(38H)	"8"
	00110111(37H)	"7"
	00110111(37H)	"7"
	00110001(31H)	"1"
DATA NAME	01010100(54H)	"T"(1BANK DATA)
BANK NO.	00000bbb	bbb = BANK NO. *11
EOX	11110111(F7H)	

7) BANK CHANGE REQUEST

Received on the MIDI channel specified for the currently selected bank.
When received, the specified bank is called up.

STATUS	11110000(F0H)	SYSTEM EXCLUSIVE
ID NO.	01000011(43H)	YAMAHA
SUB STATUS	0000nnnn	nnnn = CHANNEL NO. *1
FORMAT NO.	01111100(7CH)	CONDITION SETSETUP
BYTE COUNT	00000000(00H)	HEADER & DATA = 13 bytes
	00001101(0DH)	
HEADER	01001100(4CH)	"L"
	01001101(4DH)	"M"
	00100000(20H)	" "
	00100000(20H)	" "
	00111000(38H)	"8"
	00110111(37H)	"7"
	00110111(37H)	"7"
	00110001(31H)	"1"
DATA NAME	01010101(55H)	"U"(BANK CHANGE)
	00100000(20H)	" "
VERSION NO.	0vvvvvvv	VERSION NO. MSB
	0vvvvvvv	VERSION NO. LSB
DATA	00000bbb	bbb = BANK NO. *11
CHECKSUM	0eeeeeee	*10
EOX	11110111(F7H)	

8) SYSTEM SETUP BULK DUMP REQUEST

Received on the MIDI channel specified for the currently selected bank.
When received, the system setup data is transmitted.

STATUS	11110000(F0H)	SYSTEM EXCLUSIVE
ID NO.	01000011(43H)	YAMAHA
SUB STATUS	0010nnnn	nnnn = CHANNEL NO. *1
FORMAT NO.	01111110(7EH)	UNIVERSAL BULK DUMP
HEADER	01001100(4CH)	"L"
	01001101(4DH)	"M"
	00100000(20H)	" "
	00100000(20H)	" "
	00111000(38H)	"8"
	00110111(37H)	"7"
	00110111(37H)	"7"
	00110001(31H)	"1"
DATA NAME	01010011(53H)	"S"(SYSTEM SETUP DATA)
	00100000(20H)	" "
EOX	11110111(F7H)	

5. NOTES

*1 nnnn = 0 (Channel 1) ~ 15 (Channel 16)
*2 kkkkkkk = 0 ~ 127
*3 vvvvvvv = 0 (Note OFF), 1 ~ 127
*4 cccccc = 1 ~ 31, 64 ~ 95
*5 vvvvvvv = 0 ~ 127
*6 ppppppp = 0 (Program 1) ~ 127 (Program 128)
*7 vvvvvvv = 0 ~ 127
*8 mmmmmmm = 0 (U01) ~ 49 (U50)
*9 Depending on memory contents
*10 eeeeeee is the 2's complement of the lowest 7 bits of the sum of all header and data bytes.
*11 bbb = 1 (Bank A) ~ 4 (Bank D)
*12 Two bytes as a set expressing a PRESET, USER, or CARD memory No.

mmmmmmmm	MEMORY NO.
0 : 90	P00 : P90
91 : 140	U01 : U50
141 : 190	C01 : C50

*13 Reception channel No. of Banks A ~ D

nnnnn	CHANNEL NO.
0	OMNI ON
1 : 16	1 : 16
17	OFF

*14 Control source of Controllers 1, 2

ddddddd	CONTROL SOURCE
0	OFF
1	MOD. WHEEL
2	BREATH CONTROL
3	——
4 : 5	FOOT CONTROL : MIDI CTRL 5
31 : 32	MIDI CTRL 31 : MIDI CTRL 64 SUSTAIN PEDAL
63	MIDI CTRL 95
64	MIDI NOTE ON KEY #
65	MIDI NOTE ON VELOCITY
66	MIDI CHANNEL PRESS.

*15 Foot switch assignment

dddd	SETTING
0	BYPASS
1	TAP TENPO
2	OFF

YAMAHA [Multi-Effect Processor] Date : 11/16, 1991
Model EMP700 MIDI Implementation Chart Version : 1.0

Function ...	Transmitted	Recognized	Remarks
Basic Default Channel Changed	x x	1 - 16, off 1 - 16, off	memorised
Default Mode Messages Altered	x x **********	OMNIoff/OMNIon x x	memorised
Note Number : True voice	x **********	0 - 127 x	
Velocity Note ON Note OFF	x x	o v=0-127 x	
After Key's Touch Ch's	x x	x o	
Pitch Bender	x	x	
1 - 31 64 - 95 Control Change	x x	o o	
Prog Change : True #	x	o	*1
System Exclusive	o	o	Bulk Dump
System : Song Pos : Song Sel Common : Tune	x x x	x x x	
System :Clock Real Time :Commands	x x	x x	
Aux :Local ON/OFF :All Notes OFF Mes- :Active Sense sages:Reset	x x x x	x x o x	

Notes: *1 = For program 1 - 128, memory P00-P90, U01-U50
C01-C50 is selected.

Mode 1 : OMNI ON, POLY Mode 2 : OMNI ON, MONO o : Yes
Mode 3 : OMNI OFF, POLY Mode 4 : OMNI OFF, MONO x : No

MULTI-EFFECT PROCESSOR

EMP700

PARTS LIST

■**CONTENTS** (目次)

Notes DESTINATION ABBREVIATIONS

A	: Australian model	J	: Japanese model
B	: British model	M	: South African model
C	: Canadian model	Q	: South-east Asia model
D	: German model	U	: U.S.A. model
E	: European model	V	: General export model (110V)
F	: French model	W	: General export model (220V)
G	: Belgian model	X	: General export model
H	: North European model	Y	: Export model
I	: Indonesian model		

■ELECTRICAL PARTS（電気部品）

	Ref. No.	Part No.	Description		部品名	Remarks	ランク
*		VL379000	Circuit Board	AD	ＡＤシート	J,U,C,V EMP700	
*		VL379100	Circuit Board	AD	ＡＤシート	H,B	
		IG001390	IC	RC4558D-V	アンプＩＣ	OP AMP.	03
*		XC349A00	IC	μPC78L05J	電源ＩＣ	5V REGULATOR	
		IG130500	IC	NJM79L05A	電源ＩＣ	-5V REGULATOR	03
		XC719A00	IC	NJM7805FA	電源ＩＣ	5V REGULATOR	02
		XC720A00	IC	NJM7812FA	電源ＩＣ	12V REGULATOR	02
*		XC721A00	IC	NJM7912FA	電源ＩＣ	-12V REGULATOR	
*		XD066A00	IC	NJM78L12A	電源ＩＣ	12V REGULATOR	
		XH970A00	IC	M62021L	電源ＩＣ	RESET	04
		IG147300	IC	HD63B50P	ＣＰＵ／周辺ＩＣ	ACIA	09
		XD245A00	IC	HD63B03YP-N	ＣＰＵ／周辺ＩＣ	CPU	08
		XG517A00	IC	LC3664RL-12	メモリＩＣ	SRAM 64K	08
*		XK356A00	IC		書込済ＥＰＲＯＭ	1M EPROM	
		XE788A00	IC	YM6104	ＬＳＩ	DEQ2	11
		XG278A00	IC	PCM66P	ＩＣ	DAC	08
		XI112A00	IC	AK5339-VP	ＩＣ	ADC	15
		XI816A00	IC	YSS208	ＬＳＩ	DSPN	13
*		XJ875A00	IC	YSS218-F	ＬＳＩ	XLTM	
		IR024500	IC	TC74HC245AP	ロジックＩＣ	BUS BUFFER	07
		IR000000	IC	TC74HC00AP	ロジックＩＣ	NAND	03
		IR000050	IC	SN74HC00N	ロジックＩＣ	NAND	03
		XC628A00	IC	TC51832PL-10	メモリＩＣ	PSRAM 256K	09
		XH116A00	IC	HM65256BLP-10	メモリＩＣ	PSRAM 256K	09
		VD473200	Photo Coupler	6N137	フォトカプラ		05
		IA1015I0	Transistor	2SA1015 Y	トランジスタ		01
		IC121340	Transistor	2SC1213A D	トランジスタ		01
		IC1815I0	Transistor	2SC1815 Y	トランジスタ		01
*		VC710400	Transistor	2SC2878 B	トランジスタ		
		IG138700	Transistor Array	TD62506P	トランジスタアレイ		03
		VB481900	Diode	11ES4	ダイオード		01
		VB941200	Diode	1SS133,1SS176	ダイオード		01
		IH000870	Diode Stack	4D4B41 4A 200V	ダイオードスタック		04
		IH001120	Diode Stack	S2VB20 2A 200V	ダイオードスタック		03
*		VJ734900	LED	GL8KG26 GR	ＬＥＤ	5pcs	
		VK018900	LED	GL8HD26 RE	ＬＥＤ	PEAK(L,R),MIDI	01
		VA026000	LED Display	LN524RKS	ＬＥＤディスプレイ	MEMORY	05
		VF771900	Resistor Array	RGLE8X103J	抵抗アレイ		01
		VF773500	Resistor Array	RGLE4X103J	抵抗アレイ		01
*		VL962700	Variable Resistor	A10KX2 RK124222	ロータリーボリュウム	INPUT LEVEL L,R	
		UJ739220	Electrolytic Cap.	2200μF 16V	ケミコン		02
		UJ749220	Electrolytic Cap.	2200μF 25V	ケミコン		03
		FI383220	Ceramic Cap.	2200pF 400V	規格認定コン		01
		FR203100	Ceramic Cap.	0.1μF	規格認定コン		03
		FI383470	Ceramic Cap.	4700pF 400V	規格認定コン	H,B	01
		VC694800	Semiconductive Cera. Cap.	0.1μF 25V Z	半導体セラコン		01
		VB835000	Coil	FL5R200QNT	コイル	20μH	01
		GD900760	Coil	PLA3021A 3mm	コイル		06
		VH408900	LC Filter	LPF 20KHZ	ＬＣフィルター		05
		FZ006970	EMI Filter	LS MT Y223NB	ＬＣフィルターＥＭＩ		02
		GE300610	Ferrite Bead	BL02RN1-R62T4	フェライトビーズ		01
		QU004800	Ceramic Resonator	4MHz CSA4.00MG	セラミック振動子		03
		VH409300	Ceramic Resonator	CSA22.5792MG	セラミック振動子		02
*		VN140900	Thermistor	ERT-D2FK103S1K	サーミスタ		
		VJ557300	Push Switch	ESB-82TYPE	プッシュスイッチ	POWER	03
*		VM475900	Slide Switch	SSSU142-S06S-0	スライドスイッチ	-20dB,+4dB	
*		VM476100	Slide Switch	SSSU112-S06S-0	スライドスイッチ	MIDI OUT,THRU	
*		VK519000	DIN Jack	5P3 YKF51-50	ＤＩＮジャック２連	MIDI IN,OUT/THR	
		VB312600	Phone Jack	YKB21-5012	ホーンジャック（黒）	IN,OUT,BYPASS	02
	-- <		IC Socket	DICF-32CS-E	ＩＣソケット	(VJ532800)	
	--		Socket	IMSA-9110S-14L	ソケット	(VM657000)	
	--		Socket	IMSA-9110S-10L	ソケット	(VM686600)	
	--		Socket	IMSA-9110S-05L	ソケット	(VM686700)	
		VF821100	Connector, Card	IC3A38PS-1.27D	ＩＣカード用コネクタ	MEMORY CARD 38P	06
		VE338400	Lithium Battery	SONY/CR2032	リチュウム電池		03
		VA855400	Terminal		ＰＣ用カラゲゲ端子		01
	--		Angle Bracket, Jack		ジャック金具	(VL820500)	
	--		Heat Sink		放熱板	(VL820700)	
*		VM495200	Spacer, LED		ＬＥＤスペーサー	1pc.	
	--		Connector Assembly	6P 80L	束線 ＃８８	(VM702800)	
		VC569900	Bind Head Tapping Screw-B	A 3.0X8 FCM3BL	＋バインドＢタイト	3pcs	01
*		VC791600	Bind Head Tapping Screw-B	A 3.0X6 FCM3BL	＋バインドＢタイト	4pcs	
*		VL842500	LCD Unit		ＬＣＤユニット		
			IC	NJU6420-02	ＬＳＩ		
		VE464300	LED	TLR220 RE	ＬＥＤ		01
			LED Back-lit		ＬＥＤバックライト		
			Tact Switch	SKHUQB	タクトスイッチ		
		VC021100	Tact Switch	SKHLAC023A	タクトスイッチ		01

*New Parts（新規部品）

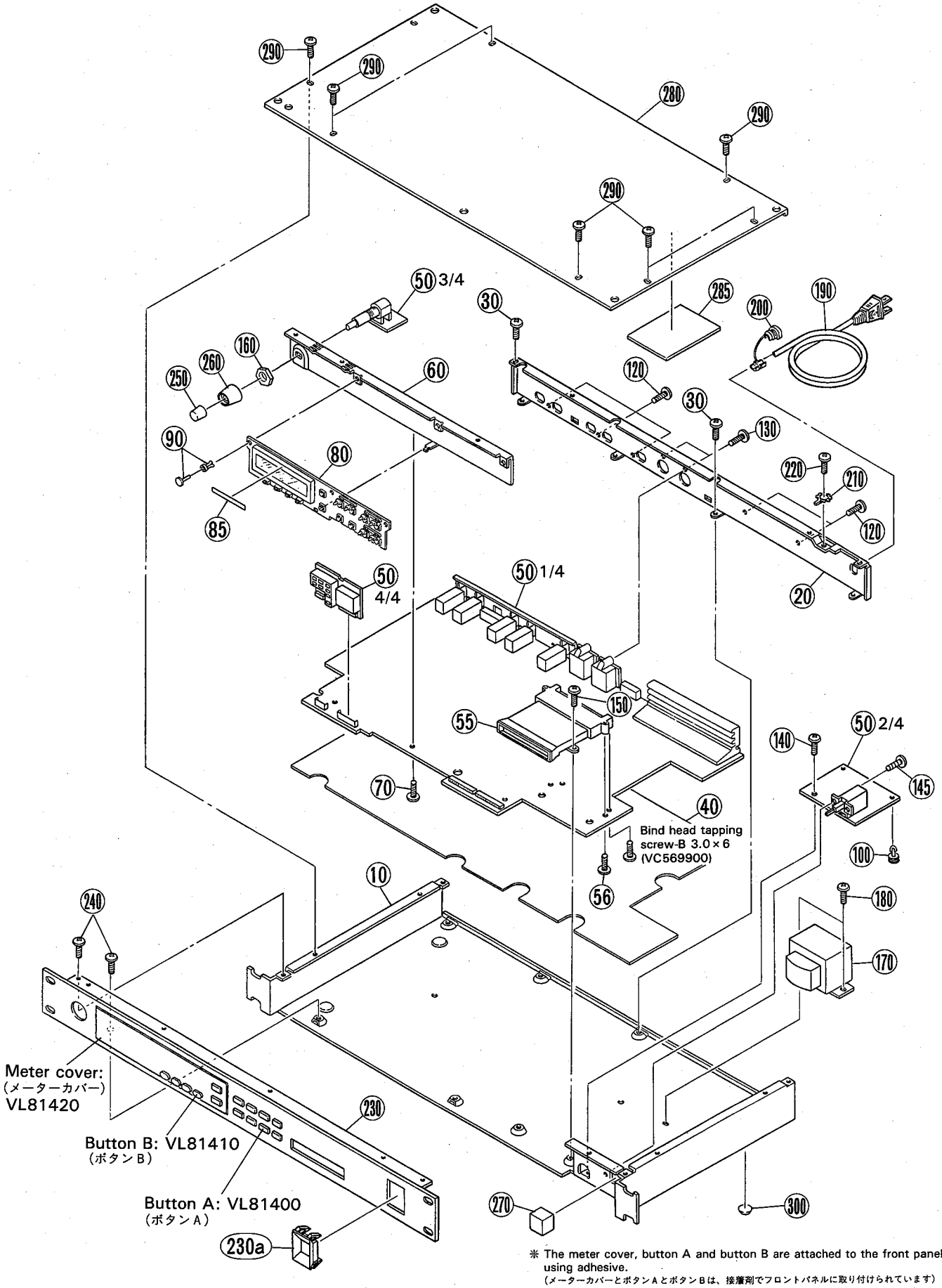
ランク：Japan only

	Ref. No.	Part No.	Description		部品名	Remarks	ランク
*		XJ769B00	Power Transformer		電源トランス	J	
* *		XJ771B00	Power Transformer		電源トランス	U,C,V	
*		XJ772B00	Power Transformer		電源トランス	H,B	
		MG002290	AC Cord	7A 125V 2m	電源コード	J	03
		VD654200	AC Cord	10A 2.44m	電源コード	U,V	05
		VD279600	AC Cord	10A 2.5m	電源コード	C	08
		VD279800	AC Cord	6A 2.5m	電源コード	H	08
		VH890200	AC Cord	10A 2.5m	電源コード	B	09

*New Parts (新規部品)

ランク : Japan only

■ OVERALL ASSEMBLY（総組立）



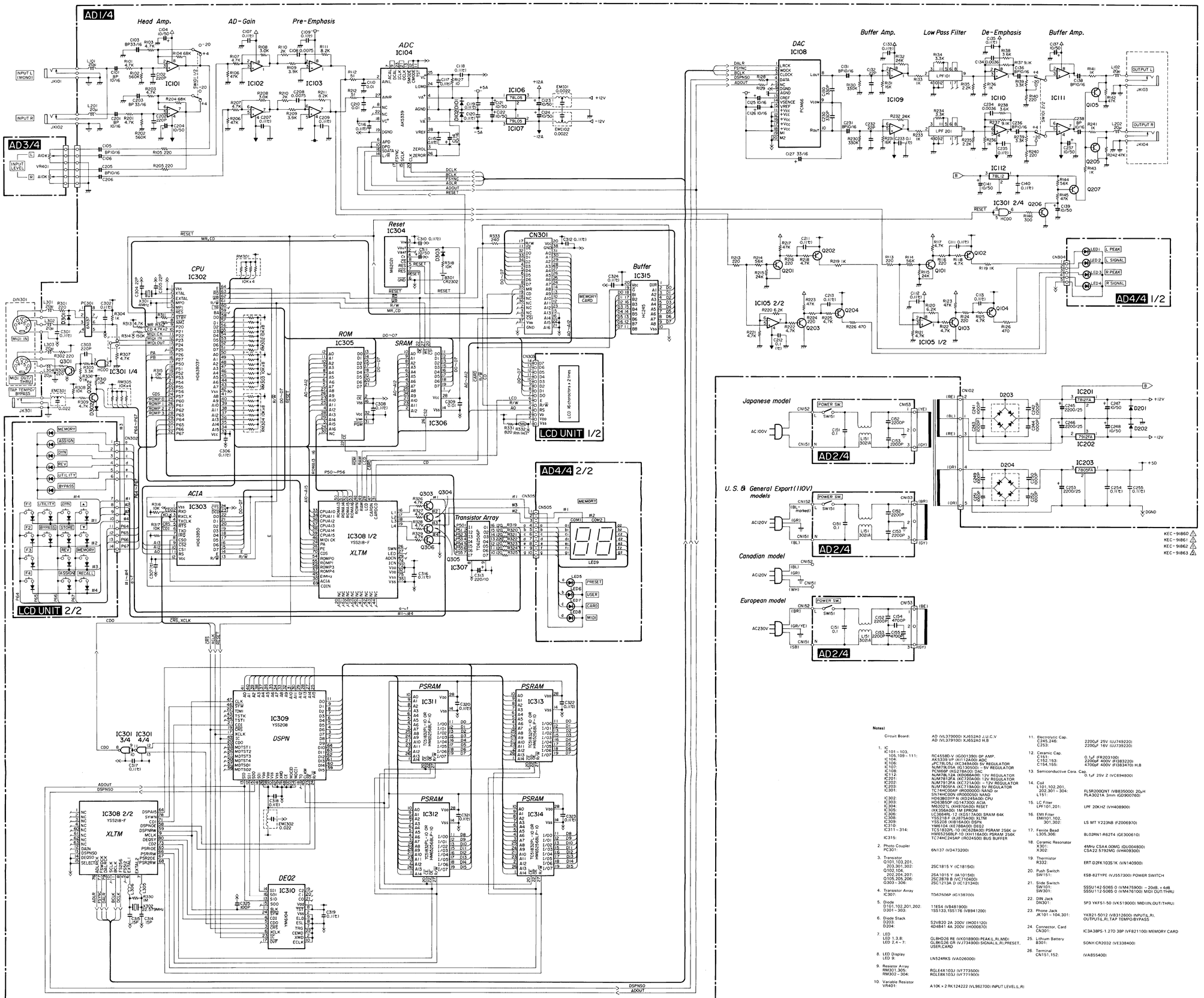
※ The meter cover, button A and button B are attached to the front panel using adhesive.
（メーターカバーとボタンAとボタンBは、接着剤でフロントパネルに取り付けられています）

	Ref. No.	Part No.	Description		部品名	Remarks	ランク
			<Overall Assembly>		<総組立>	EMP700	
*	10	VL810900	Bottom Cover		ボトムカバー		
*	20	VL811000	Rear Panel		リアパネル	J	
*	20	VL811100	Rear Panel		リアパネル	U,V	
*	20	VL997100	Rear Panel		リアパネル	C	
*	20	VL811200	Rear Panel		リアパネル	H,B	
*	30	VC791600	Bind Head Tapping Screw-B	A 3.0X6 FCM3BL	+バインドBタイト	6pcs	
*	40	VL812700	Isolation Sheet		絶縁シート		
*	50	VL379000	Circuit Board	AD	ADシート	J,U,C,V	
*	50	VL379100	Circuit Board	AD	ADシート	H,B	
*	55	VN303700	Card Guide		カードガイド		
	56	VC569900	Bind Head Tapping Screw-B	A 3.0X8 FCM3BL	+バインドBタイト	2pcs	01
*	60	VL820600	Sub Panel		サブパネル		
*	70	VC791600	Bind Head Tapping Screw-B	A 3.0X6 FCM3BL	+バインドBタイト	3pcs	
*	80	VL842500	LCD Unit		LCDユニット		
*	85	VN211300	LCD Spacer		LCDスペーサー	1pc.	
	85	--	LCD Spacer		LCDスペーサー	(VN21130) 1pc.	
	90	CB068880	Plastic Rivet		プラスチックリベット	3pcs	01
*	100	VM502800	Spacer	MPS-04	ミニカードスペーサー	2pcs	
*	120	VC791600	Bind Head Tapping Screw-B	A 3.0X6 FCM3BL	+バインドBタイト	5pcs	
	130	VC569900	Bind Head Tapping Screw-B	A 3.0X8 FCM3BL	+バインドBタイト	2pcs	01
*	140	VC791600	Bind Head Tapping Screw-B	A 3.0X6 FCM3BL	+バインドBタイト	1pc.	
	145	EG330410	Bind Head Screw	A 3.0X6 FCM3BL	+バインド小ネジ	2pcs	01
*	150	VC791600	Bind Head Tapping Screw-B	A 3.0X6 FCM3BL	+バインドBタイト	2pcs	
	160	VC364900	Hexagonal Nut	φ9.0 FCM3BL	特殊六角ナット	1pc.	01
*	170	XJ769B00	Power Transformer		電源トランス	J	
*	170	XJ771B00	Power Transformer		電源トランス	U,C,V	
*	170	XJ772B00	Power Transformer		電源トランス	H,B	
	180	VC569900	Bind Head Tapping Screw-B	3.0X8 FCM3BL	+バインドBタイト	2pcs	01
	190	MG002290	AC Cord	7A 125V 2m	電源コード	J	03
	190	VD654200	AC Cord	10A 2.44m	電源コード	U,V	05
	190	VD279600	AC Cord	10A 2.5m	電源コード	C	08
	190	VD279800	AC Cord	6A 2.5m	電源コード	H	08
	190	VH890200	AC Cord	10A 2.5m	電源コード	B	09
	200	CB068630	Cord Strain Relief	SR-3P-4	コードストッパー	J	01
	200	VD705000	Cord Strain Relief	SR-5KN-4	コードストッパー	U,V	02
	200	CB806850	Cord Strain Relief	SR-6N3-4	コードストッパー	C	02
	200	CB032840	Cord Strain Relief	SR-5N-4	コードストッパー	H,B	01
	210	LA003690	Lug Terminal		ラグ端子	U,C,H,B,V	01
	220	EP600780	Bind Head Tapping Screw-B	4.0X8 FCM3BL	+バインドBタイト	U,C,H,B,V(1pc.)	01
*	230	VL810700	Front Assembly		フロントAss'y		
*	230a	VL813000	Escutcheon, Power Switch		PSWエスカッション		
*	240	VC791600	Bind Head Tapping Screw-B	A 3.0X6 FCM3BL	+バインドBタイト	6pcs	
*	250	VL821700	Knob, Volume		VRツマミ(内)	INPUT LEVEL/L	
*	260	VL821800	Knob, Volume		VRツマミ(外)	INPUT LEVEL/R	
*	270	VL812900	Knob, Power Switch		PSWツマミ	POWER	
*	280	VL811300	Top Cover		トップカバー		
*	285	VM919400	Isolation Sheet-S		絶縁シート(S)		
*	290	VC791600	Bind Head Tapping Screw-B	A 3.0X6 FCM3BL	+バインドBタイト	8pcs	
	300	CB037120	Foot		スベリ座	4pcs	01

*New Parts (新規部品)

ランク : Japan only

■ EMP700 OVERALL CIRCUIT DIAGRAM



Notes)

Circuit Board: AD (VL379000) X-6252A0 J,U,C,V
AD (VL379100) X-6252A0 H,B

1. IC
   IC101 – 103, 105, 109 – 111: RC4558D-V (IGO01390) OP AMP.
   IC104: AK5339-VP (X1132A000) ADC
   IC105: μPC78L05J (XC349A00) 5V REGULATOR
   IC106: NJM79L05A (X1340500) – 5V REGULATOR
   IC107: NJM7905A (X1340600) –5V
   IC108: NJM78L12A-(XB0664A0) 12V REGULATOR
   IC201: NJM7812FA (IKC720A00) 12V REGULATOR
   IC202: NJM7912FA (IKC721A00) –12V REGULATOR
   IC203: NJM7805FA (IKC719A00) 5V REGULATOR
   IC301: TC74HC00AP (IR000000) NAND or SN74HC00N (IR000050) NAND
   IC302: HD63B03Y-N (XD2454A00) CPU
   IC303: HD63850P (IG147300) ACIA
   IC304: M52021L (XH970A00) RESET
   IC305: (XK356A00) 1M EPROM
   IC306: LC3664ML-12 (XG517A00) SRAM 64K
   IC308: YSS218-F (XJ875A00) XLTM
   IC309: YSS208 (XB164A00) DSPN
   IC310: TC51V1664 (KE788A00) DE02
   IC311 – 314: HM538253BLP-10 (XC628A00) PSRAM 256K or HM65256BLP-10 (XH116A00) PSRAM 256K
   IC315: TC74HC245AP (IR024500) BUS BUFFER
2. Photo Coupler PC301: 6N137 (VD473200)
3. Transistor Q101, 103, 201, 203, 301, 302: 2SC1815 Y (IC181510)
   Q102, 104, 202, 204, 207: 2SA1015 Y (IA101510)
   Q105, 205, 206: 2SC2878 B (VC710400)
   Q303 – 306: 2SC1213A D (IC121340)
4. Transistor Array IC307: TD62506P (IG138700)
5. Diode D101, 102, 201, 202: 1SS133, 1SS176 (VB941200)
   D301 – 303: 11ES4 (VB481900)
6. Diode Stack D203: S2VB20 2A 200V (IH001120)
   D204: 4D4B41 4A 200V (IH000870)
7. LED LED 1, 3, 8: GL8HD26 RE (VK018900) PEAK(L,R),MID)
   LED 2, 4 – 7: GL8KD26 GR (VJ734900) SIGNAL(L,R),PRESET, USER,CARD
8. LED Display LED 9: LN524RKS (VA026000)
9. Resistor Array RM301, 305: RGLE6X103J (VF773500)
   RM302 – 304: RGLE8X103J (VF771900)
10. Variable Resistor VR401: A10K × 2 RK124222 (VL962700) INPUT LEVEL(L,R)
11. Electrolytic Cap. C245, 246: 2200μF 25V (UJ749220)
    C253: 2200μF 16V (UJ739220)
12. Ceramic Cap. C151: 0.1μF (FR203100)
    C152, 153: 2200pF 400V (FI383220)
    C154, 155: 4700pF 400V (FI383470) H,B
13. Semiconductive Cera. Cap. 0.1μF 25V Z (VC694800)
14. Coil L101, 102, 201, 202, 301 – 304: FL5R200QNT (VB835000) 20μH
    L151: PLA3021A 3mm (GD900760)
15. LC Filter LPF101, 201: LPF 20KHZ (VH408900)
16. EMI Filter EMI101, 102, 301, 302: LS MT Y223NB (FZ006970)
17. Ferrite Bead L305, 306: BL02RN1-R62T4 (GE300610)
18. Ceramic Resonator X301: 4MHz CSA4.00MG (QU004800)
    X302: CSA22.5792MG (VH409300)
19. Thermistor R332: ERT-D2FK103S1K (VN140900)
20. Push Switch SW151: ESB-82TYPE (VJ557300) POWER SWITCH
21. Slide Switch SW101: SSSU142-S065 0 (VM475900) – 20dB, + 4dB
    SW301: SSSU112-S065 0 (VM476100) MID OUT/THRU
22. DIN Jack DN301: 5P3 YKF51-50 (VK519000) MID(IN,OUT/THRU)
23. Phone Jack JK101 – 104, 301: YK821-5012 (VB312600) INPUT(L,R), OUTPUT(L,R),TAP TEMPO/BYPASS
24. Connector, Card CN301: IC3A38PS-1.27D 38P (VF821100) MEMORY CARD
25. Lithium Battery B301: SONY:CR2032 (VE338400)
26. Terminal CN151, 152: (VA855400)